

HP Patton X2 (HP SCH P/N:675886-000)

BTX(213.3 mm X 266.7 mm)

(MS-7782 0B)

| HP P/N | Description |
|------------|-------------|
| 675885-001 | PCA, Patton |
| 675886-000 | SCH, Patton |
| 675887-001 | PCB, Patton |

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CPU:

INTEL - Sandy or Ivy Bridge LGA 1155

System Chipset:

INTEL-IBEXPEAK PCH-H61

OnBoard Chipset:

AZALIA Codec: ALC 221

LAN: Boradcom BCM57788 10/100/1000 NIC

SIO: Nuvoton NPCD379H

PCIe to PCI Bridge: ASM1083

Flash ROM: 64 Mb

Main Memory:

DDR3 (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PCI Slot * 2

PWM:

Controller: NCP81005

Controller: NCP5230MNTWG

Controller: TPS51220

Controller: NCP1587DR2G

Other:

SATA(SATA2-300MB/s) *2

USB2.0 *10 (Rear*4 Front*4 Internal *2)

DVI-D*1

VGA PORT *1

PRINT Header *1

COM PORT *1

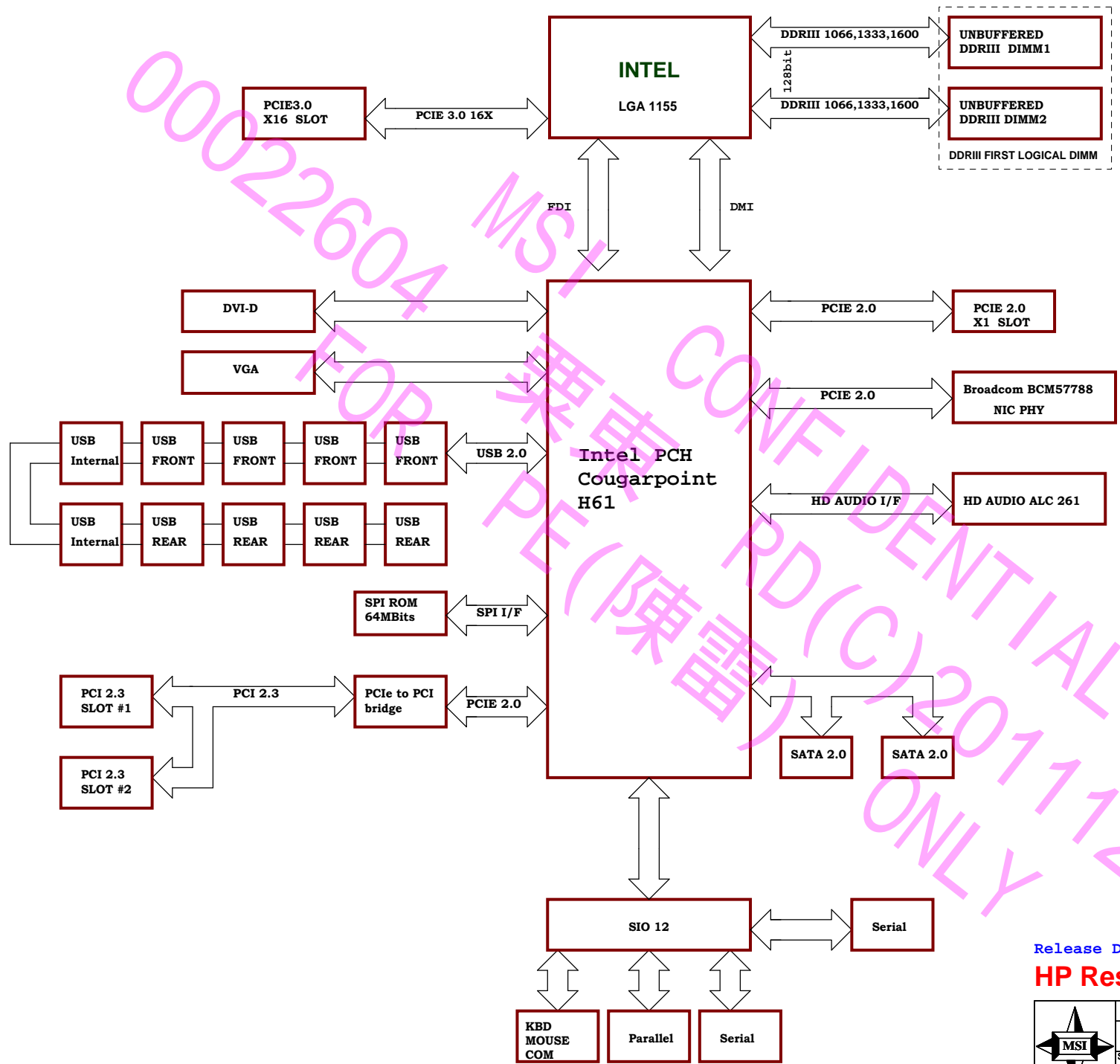
COM Header *1

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| Block Diagram | | |
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DDR DIMM Config.

| DEVICE | ADDRESS | CLOCK |
|----------------|-----------|--------------------------------------|
| | | |
| DIMM 1 CH-A | 10100000B | MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1 |
| | | |
| DIMM 3 CH-B | 10100010B | MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1 |

PCI Config.

| DEVICE | MCP1 INT Pin | REQ#/GNT# | IDSEL | CLOCK |
|--------------------------|--|------------------------|-------|------------------|
| PCI Slot 1 | PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D | PCI_REQ0# PCI_GNT0# | AD16 | CLK33M_PCI_SLOT1 |
| PCI Slot 2 | PCI_INT#B PCI_INT#C PCI_INT#D PCI_INT#A | PCI_REQ1# PCI_GNT1# | AD17 | CLK33M_PCI_SLOT2 |
| SIO | | | | CLK33M_SIO |
| PCIe to PCI Bridge | | | | CK_ASM_PCI33M |

USB MAPPING


| Controller | Port | Destination | Fuse | Bulk Cap | OC# |
|------------|---------|---------------------------------|------|----------|-----|
| EHCI #1 | Port 0 | Front I/O (P24) | SW | YES | 3 |
| | Port 1 | Front I/O (P24) | | | |
| | Port 2 | Media (P150) | SW | YES | 0 |
| | Port 3 | Media (P150) | | | |
| | Port 4 | Front I/O (P25) | SW | YES | 3 |
| | Port 5 | Front I/O (P25) | | | |
| | Port 6 | USB Port 6 is disabled for H61 | | | |
| | Port 7 | USB Port 7 is disabled for H61 | | | |
| EHCI #2 | Port 8 | Lan +USB | SW | YES | 6 |
| | Port 9 | Lan +USB | | | |
| | Port 10 | Rear USB x2 | SW | YES | 5 |
| | Port 11 | Rear USB x2 | | | |
| | Port 12 | USB Port 12 is disabled for H61 | | | |
| | Port 13 | USB Port 13 is disabled for H61 | | | |

PCI RESET DEVICE

| IBEXPEAK | |
|-------------|--------------------------|
| Signals | Target |
| PCI_RST# | PCI SLOT1 (J20) |
| PCI_RST# | PCI SLOT2 (J21) |
| | |
| PE_X16_RST# | PCI-E SLOT X16 (J41) |
| PE_X1_RST# | PCI-E SLOT X1 (J31) |
| PE_LAN_RST# | LAN (U10) |
| PE_PCI_RST# | PCIe to PCI Bridge (U12) |

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| Pin | Default Function / Alternate Functions | Buffer Type | Buffer Power Wells | Motherboard Function |
|-----|--|--|--------------------|----------------------|
| 1 | CLAMP_CTRL | OD ₆ | VS _{B3} | BLEED OFF CIRCUIT |
| 2 | SLP_S4# | IN _{T04} | VS _{B3} | SLP_S4# |
| 3 | SLP_S5# | IN _{T04} | VS _{B3} | SLP_S5# |
| 4 | SLP_S3# | IN _{T04} | VS _{B3} | SLP_S3# |
| 5 | SIOPME# | OD ₆ , O ₄₈ | VS _{B3} | RI# |
| 6 | RSMRST# | O ₃₆ | VS _{B3} | RSMRST# |
| 7 | PME_IN# | IN _{T0} | VS _{B3} | PME status |
| 8 | BLINK_GR | O _{20/30} | VS _{B3} | Power LED driver |
| 9 | COLOR | O _{30/30} | VS _{B3} | Power LED driver |
| 10 | VSS | I | GND | GND |
| 11 | PWRGD_OUT | OD ₆ | VS _{B3} | PWRGD_140ms |
| 12 | PS_ON# | OD ₆ | VS _{B3} | PS_ON# |
| 13 | TACH1 | IN _{T0} | VDD3 | SYS_FAN_TACH |
| 14 | CLOCKI32 | IN _{T0} | VS _{B3} | SUS_CLK_IO |
| 15 | 3V_AUX_SLOT_ON | O ₄₈ | VS _{B3} | 3V_AUX_SLOT_ON |
| 16 | VS _{B3} | I | PWR | VS _{B3} |
| 17 | VCORF | I | N/A | VCORF |
| 18 | LDRQ# | O _{PC1} | VDD3 | LDRQ# |
| 19 | LAD3 | IN _{PC1} /O _{PC1} | VDD3 | LAD3 |
| 20 | LAD0 | IN _{PC1} /O _{PC1} | VDD3 | LAD0 |
| 21 | LAD2 | IN _{PC1} /O _{PC1} | VDD3 | LAD2 |
| 22 | VSS | I | PWR | GND |
| 23 | LAD1 | IN _{PC1} /O _{PC1} | VDD3 | LAD1 |
| 24 | SER_IRQ | IN _{PC1} /O _{PC1} | VDD3 | SERIRQ |
| 25 | PCI_RESET# | IN _{PC1} | VDD3 | PLTRST# |
| 26 | PCI_CLK | IN _{PC1} | VDD3 | 33MHz |
| 27 | LFRANE# | IN _{PC1} | VDD3 | LFRANE# |
| 28 | VS _{B3} | I | PWR | VS _{B3} |
| 29 | GPRST3# | O ₁₄ | VS _{B3} | PCIE_X16 RESET# |
| 30 | INTRUDER# | IN _{T0} | V _{BAT} | HOOD_SENSE# |
| 31 | 5V_USB_CTRL | O ₄₈ | VS _{B3} | 5V_USB_EN |
| 32 | HDLOCK# | OD ₁₂ | VDD3 | HOOD_LOCK# |
| 33 | GPI001 | IN _{T0} /OD ₆ /O ₄₈ | VS _{B3} | |
| 34 | HDUNLOCK# | OD ₁₂ | VDD3 | HOOD_UNLOCK# |
| 35 | HD_LED_IN# | IN _{T0} | VDD3 | Hard Drive LED Input |
| 36 | CPU_PRSTNT1# | IN _{T0L} | V _{BAT} | CPU detection |
| 37 | VBAT | I | PWR | |

| | | | | |
|----|------------------|--|------------------|-----------------------|
| 38 | 12V_VSB_COMP | IN _{COMP2} | VS _{B3} | |
| 39 | COMP_IN3 | IN _{COMP3} | VS _{B3} | |
| 40 | COMP_IN1 | IN _{COMP1} | VS _{B3} | 5V voltage monitor |
| 41 | COMP_IN2 | IN _{COMP2} | VS _{B3} | 12V voltage monitor |
| 42 | AVCC | I | PWR | AVCC |
| 43 | AD1 | IN _{PC1} /O _{PC1} | VDD3 | AD1 |
| 44 | AD2 | IN _{PC1} /O _{PC1} | VDD3 | AD2 |
| 45 | AD3 | IN _{PC1} /O _{PC1} | VDD3 | AD3 |
| 46 | FSPI_STR | IN _{T0} | AVCC | FSPI_STR |
| 47 | AGND | I | GND | AGND |
| 48 | PWBTOUT# | IN _{T04} | VLPS | PWBTOUT# |
| 49 | PWBTIN# | IN _{T04} | VLPS | PWBTIN# |
| 50 | LPS_WAKE | IN _{T0} | VLPS | LPS_WAKE |
| 51 | LPS_PHY# | O ₄₈ | VLPS | LPS_PHY# |
| 52 | LPS_ON# | O ₄₈ | VLPS | LPS_ON# |
| 53 | VLPS | I | PWR | VLPS |
| 54 | VTT | I | PWR | VTT |
| 55 | THERMTRIP# | IN _{AGTL} | VTT | THERMTRIP# |
| 56 | TSI_SCL | IN _{T0} /O _{T01} | VTT | TSI_SCL |
| 57 | PROCHOT1# | IN _{AGTL} /OD _{AGTL24} | VTT | PROCHOT1# |
| 58 | PECI | IN _{PE1} /O _{PE1} | VTT | PECI |
| 59 | PROCHOT2# | IN _{AGTL} /OD _{AGTL24} | VTT | PROCHOT2# |
| 60 | VSS | I | PWR | GND |
| 61 | PWM2 | OD ₁₂ /O _{6/12} | VDD3 | FANPWM_REAR |
| 62 | HMSCL | IN ₃₄ /OD ₆ | VS _{B3} | HMSCL |
| 63 | PWM1 | OD ₁₂ /O _{6/12} | VDD3 | FANPWM_FRONT |
| 64 | HMSDA | IN ₃₄ /OD ₆ | VS _{B3} | HMSDA |
| 65 | HD_LED_OUT | OD ₁₆ | VS _{B3} | Hard Drive LED Output |
| 66 | WAKE_OUT# | OD ₁₂ /O _{6/12} | VS _{B3} | Wake Disable Output |
| 67 | GPI015(EV6#) | IN _{T0} | VS _{B3} | PCI_Express_Wake# |
| 68 | AMP_ON | O ₄₈ | VS _{B3} | AMP_ON |
| 69 | AMP_ON# | O ₄₈ | VS _{B3} | AMP_ON# |
| 70 | GPRST2# | O _{14/14} | VS _{B3} | PE_RST#_OUT |
| 71 | 12V_PG_25MS | OD ₆ | VS _{B3} | 12V_PG_25MS |
| 72 | KBDNST# | IN _{T0} /OD ₁₄ | VDD3 | KBDNST# |
| 73 | AUDIO_BEEP | O ₄₈ | VS _{B3} | DIAG Beep |
| 74 | TACH2 | IN _{T0} | VDD3 | TACH2 |
| 75 | VS _{B3} | I | PWR | VS _{B3} |
| 76 | KBDAT | IN _{T0} /OD ₁₄ | VDD3 | KBDAT |
| 77 | MDAT | IN _{T0} /OD ₁₄ | VDD3 | MSDATA |
| 78 | SLIN_ASTRB# | OD ₁₄ /O _{14/14} | VDD3 | RSLIN# |
| 79 | KBCLK | IN _{T0} /OD ₁₄ | VDD3 | KBCLK |
| 80 | MCLK | IN _{T0} /OD ₁₄ | VDD3 | MCLK |
| 81 | PD3 | IN _{T0} /O _{14/14} | VDD3 | PD3 |
| 82 | PD4 | IN _{T0} /O _{14/14} | VDD3 | PD4 |

| | | | | |
|-----|------------------|--------------------------------------|------------------|------------------|
| 83 | INIT# | OD ₁₄ /O _{14/14} | VDD3 | INIT# |
| 84 | VSS | I | PWR | GND |
| 85 | PD1 | IN _{T0} /O _{14/14} | VDD3 | PD1 |
| 86 | PD6 | IN _{T0} /O _{14/14} | VDD3 | PD6 |
| 87 | PD0 | IN _{T0} /O _{14/14} | VDD3 | PD0 |
| 88 | PD2 | IN _{T0} /O _{14/14} | VDD3 | PD2 |
| 89 | PD7 | IN _{T0} /O _{14/14} | VDD3 | PD7 |
| 90 | PD5 | IN _{T0} /O _{14/14} | VDD3 | PD5 |
| 91 | STB_WWRITE# | OD ₁₄ /O _{14/14} | VDD3 | RSTB# |
| 92 | ERR# | IN _T | VDD3 | RERR# |
| 93 | VS _{B3} | I | PWR | VS _{B3} |
| 94 | AFD_DSTRB# | OD ₁₄ /O _{14/14} | VDD3 | RAFD# |
| 95 | PE | IN _T | VDD3 | RPE |
| 96 | GA20 | IN _{T0} /O _{14/14} | VDD3 | GA20 |
| 97 | ACK# | IN _T | VDD3 | RACK# |
| 98 | SLCT | IN _T | VDD3 | RSLCT |
| 99 | BUST_WAIT# | IN _T | VDD3 | RBUSY |
| 100 | TACH3 | INTS | VDD3 | TACH3 |
| 101 | SMB1SDA | SW ₃₄ | VDD3 | SMB_DATA_MAIN |
| 102 | PWRGD_PS | IN _{T04} | VS _{B3} | PWROK_PS |
| 103 | SMB2SDA | SW ₃₄ | VDD3 | SMB_DATA_RESUME |
| 104 | PWRGD_O2# | OD ₆ | VS _{B3} | PWRGD_50MS# |
| 105 | PWM3# | OD ₁₂ /O _{6/12} | VDD3 | PSU-FANPWM |
| 106 | 5V_USB_MAIN# | OD ₆ | VS _{B3} | 5V_USB_MAIN# |
| 107 | PWRGD_O1 | OD ₆ | VS _{B3} | PWRGD_30MS |
| 108 | VSS | I | PWR | GND |
| 109 | SMB1SCL | SW ₃₄ | VDD3 | SMB_CLK_MAIN |
| 110 | SMI# | OD ₆ | VDD3 | IO_SMI# |
| 111 | SMB2SDL | SW ₃₄ | VDD3 | SMB_CLK_RESUME |
| 112 | DSR1# | IN _{T0} | VDD3 | DSRA# |
| 113 | RI1# | IN _{T0} | VDD3 | RIA# |
| 114 | CTS1# | IN _{T0} | VDD3 | CTSA# |
| 115 | DCD1# | IN _{T0} | VDD3 | DCDA# |
| 116 | SIN1 | IN _{T0} | VDD3 | SINA |
| 117 | RTS1# | O ₄₈ | VDD3 | RTSA# |
| 118 | DTR#_BOUT1 | O ₄₈ | VDD3 | DTRA# |
| 119 | SOUT1 | O ₄₈ | VDD3 | SOUTA |
| 120 | DCD2# | IN _{T0} | VDD3 | DCDB# |
| 121 | SOUT2 | O ₄₈ | VDD3 | SOUTB |
| 122 | VS _{B3} | I | PWR | VS _{B3} |
| 123 | DTR#_BOUT2 | O ₄₈ | VDD3 | DTRB# |
| 124 | RI2# | IN _{T0} | VDD3 | RIE# |
| 125 | RTS2# | O ₄₈ | VDD3 | RTSB# |
| 126 | SIN2 | IN _{T0} | VDD3 | SINB |
| 127 | DSR2# | IN _{T0} | VDD3 | DSRB# |
| 128 | CTS2# | IN _{T0} | VDD3 | CTSB# |

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| | | SIO GPIO Table | |
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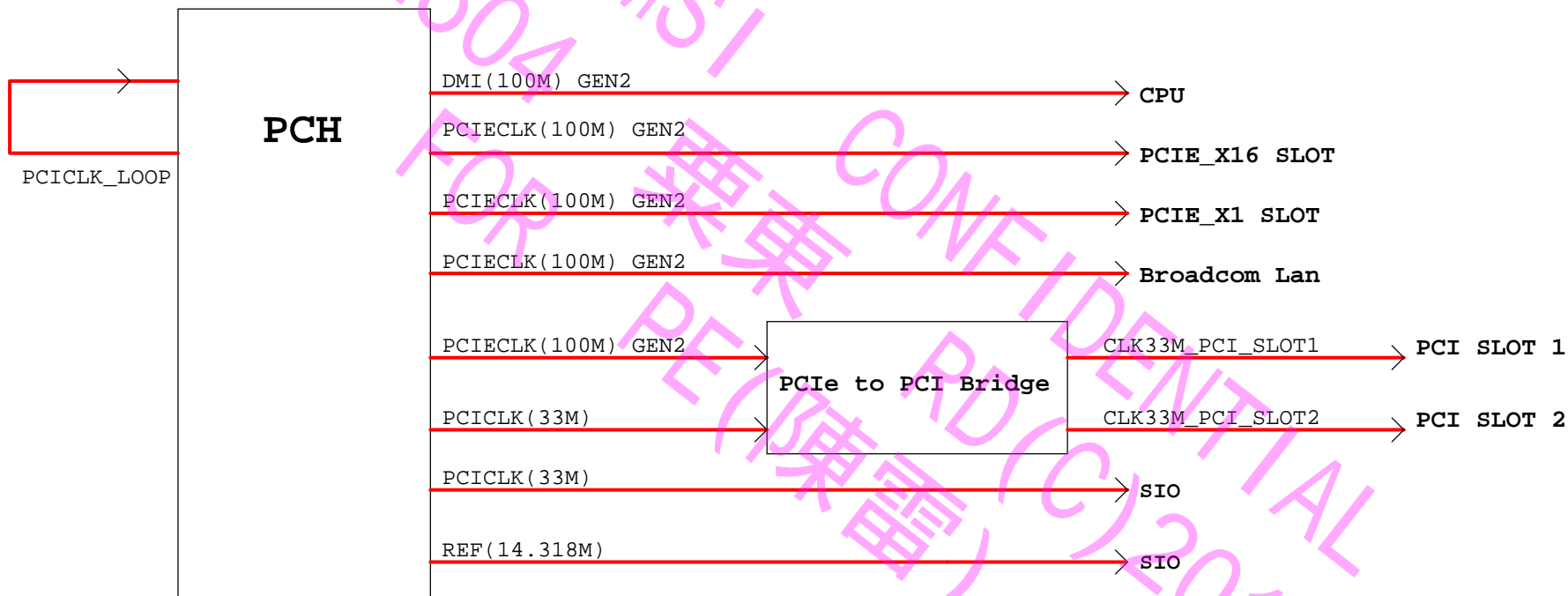
| Name | Type | Tolerance | Power Well | Native or GP | Patton Function |
|-------------------------------------|------|-----------|------------|--------------|--------------------|
| GPIO0 | IO | 3.3 V | Core | GPI | FRONT_USB_P24_DET# |
| GPIO1 | IO | 3.3 V | Core | GPI | RESTORE_PCH# |
| GPIO2 | IOD | 5 V | Core | Native | PIRQE# |
| GPIO3 | IOD | 5 V | Core | Native | PIRQ_F# |
| GPIO4 | IOD | 5 V | Core | Native | PIRQ_G# |
| GPIO5 | IOD | 5 V | Core | Native | PIRQ_H# |
| GPIO6 | IO | 3.3 V | Core | GPI | IO_SMI# |
| GPIO7 | IO | 3.3 V | Core | GPI | MXM_TH_ALERT# |
| GPIO8 | IO | 3.3 V | Suspend | GPI | BRD_ID2 |
| GPIO9 | IO | 3.3 V | Suspend | Native | USB_OCP#_REAR |
| GPIO10 | IO | 3.3 V | Suspend | Native | USB_OCP#_LAN |
| GPIO11 | IO | 3.3 V | Suspend | GPO | PWR_COMA_CFG1 |
| GPIO12 | IO | 3.3 V | Suspend | Native | LAN_DISABLE# |
| GPIO13 | IO | 3.3 V | Suspend | GPI | INT_USB_P151_DET# |
| GPIO14 | IO | 3.3 V | Suspend | Native | OC7# |
| GPIO15 | IO | 3.3 V | Suspend | GPO | Reserved |
| GPIO16 | IO | 3.3 V | Core | GPI | HOOD_SW_DET# |
| GPIO17 | IO | 3.3 V | Core | GPO | Reserved |
| GPIO18 (Mobile Only) | IO | 3.3 V | Core | Native | N/A |
| GPIO19 | IO | 3.3 V | Core | GPI | Reserved |
| GPIO20 | IO | 3.3 V | Core | Native | PCIECLKRQ2# |
| GPIO21 | IO | 3.3 V | Core | GPI | FRONT_AUD_DET# |
| GPIO22 | IO | 3.3 V | Core | GPI | INT_USB_P150_DET# |
| GPIO23 | IO | 3.3 V | Core | Native | LDRQ1# |
| GPIO24 | IO | 3.3 V | Suspend | GPI | BRD_REV1 |
| GPIO25 (Mobile Only) | IO | 3.3 V | Suspend | Native | N/A |
| GPIO26 (Mobile Only) | IO | 3.3 V | Suspend | Native | N/A |
| GPIO27 | IO | 3.3 V | Deep Sleep | GPI | DSW_WOL_WAKE |
| GPIO28 | IO | 3.3 V | Suspend | GPO | RSTBTN_EN# |
| GPIO29 | IO | 3.3 V | Suspend | Native | SLP_LAN# |
| GPIO30 | IO | 3.3 V | Deep Sleep | Native | SUS_WARN# |
| GPIO31 | IO | 3.3 V | Deep Sleep | GPI | Reserved |
| GPIO32 (not available in mobile) | IO | 3.3 V | Core | GPI | STD_PS_DET# |
| GPIO33 | IO | 3.3 V | Core | GPI | PRNTR_DET# |
| GPIO34 | IO | 3.3 V | Core | GPI | HOOD_LOCK_DET |
| GPIO35 | IO | 3.3 V | Core | GPI | BRD_REV0 |

| | | | | | |
|-------------------------|----|-------|---------|-------------------------|--------------------|
| GPIO36 | IO | 3.3 V | Core | GPO | PWR_COMA_CFG0 |
| GPIO37 | IO | 3.3 V | Core | GPO | PWR_COMB_CFG0 |
| GPIO38 | IO | 3.3 V | Core | GPI | CHASSIS_ID0 |
| GPIO39 | IO | 3.3 V | Core | GPI | BRD_ID1 |
| GPIO40 | IO | 3.3 V | Suspend | Native | OC1# |
| GPIO41 | IO | 3.3 V | Suspend | Native | OC2# |
| GPIO42 | IO | 3.3 V | Suspend | Native | USB_OCP#_FRONT |
| GPIO43 | IO | 3.3 V | Suspend | GPI | PASSWORD_EN |
| GPIO44 | IO | 3.3 V | Suspend | GPI | DWR_STATUS |
| GPIO45 | IO | 3.3 V | Suspend | GPI | PCIE_RISER# |
| GPIO46 | IO | 3.3 V | Suspend | GPI | PCI_RISER# |
| GPIO47 (Mobile Only) | IO | 3.3 V | Suspend | Native | N/A |
| GPIO48 | IO | 3.3 V | Core | GPI | CHASSIS_ID1 |
| GPIO49 | IO | 3.3 V | Core | GPI | BRD_ID0 |
| GPIO50 | IO | 5.0 V | Core | Native | REQ1# |
| GPIO51 | IO | 3.3 V | Core | Native | GNT1# |
| GPIO52 | IO | 5.0 V | Core | Native | REQ2# |
| GPIO53 | IO | 3.3 V | Core | Native | GNT2# |
| GPIO54 | IO | 5.0 V | Core | GPI | BOOT_BLK_EN# |
| GPIO55 | IO | 3.3 V | Core | GPO | LPC_DISABLE# |
| GPIO56 (Mobile Only) | IO | 3.3 V | Suspend | Native | N/A |
| GPIO57 | IO | 3.3 V | Suspend | GPI | PWR_SER_DET# |
| GPIO58 | IO | 3.3 V | Suspend | Native | SML1CLK |
| GPIO59 | IO | 3.3 V | Suspend | Native | USB_OCP#_MEDIA |
| GPIO60 | IO | 3.3 V | Suspend | GPO | MXM_PWR_LEVEL |
| GPIO61 | IO | 3.3 V | Suspend | Native | SUS_STAT# |
| GPIO62 | IO | 3.3 V | Suspend | Native | SUSCLK |
| GPIO63 | IO | 3.3 V | Suspend | Native | SLP_S5# |
| GPIO64 | IO | 3.3 V | Core | Native | CLKOUTFLEX0 |
| GPIO65 | IO | 3.3 V | Core | Native | CLKOUTFLEX1 |
| GPIO66 | IO | 3.3 V | Core | Native | CLKOUTFLEX2 |
| GPIO67 | IO | 3.3 V | Core | Native | CLKOUTFLEX3 |
| GPIO68 | IO | 3.3 V | Core | GPI | FRONT_USB_P25_DET# |
| GPIO69 | IO | 3.3 V | Core | GPI | COMM_B_DET# |
| GPIO70 | IO | 3.3 V | Core | GPI | BOOT_BLK_REC# |
| GPIO71 | IO | 3.3 V | Core | GPO | GFX_RST# |
| GPIO72 | IO | 3.3 V | Suspend | Native (Mobile Only) | BATLOW# |
| GPIO73 (Mobile Only) | IO | 3.3 V | Suspend | Native | N/A |
| GPIO74 | IO | 3.3 V | Suspend | GPO | PWR_COMB_CFG1 |
| GPIO75 | IO | 3.3 V | Suspend | Native | SML1DATA |

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| Size Custom | Document Description PCH GPIO Table | | Rev X2 |
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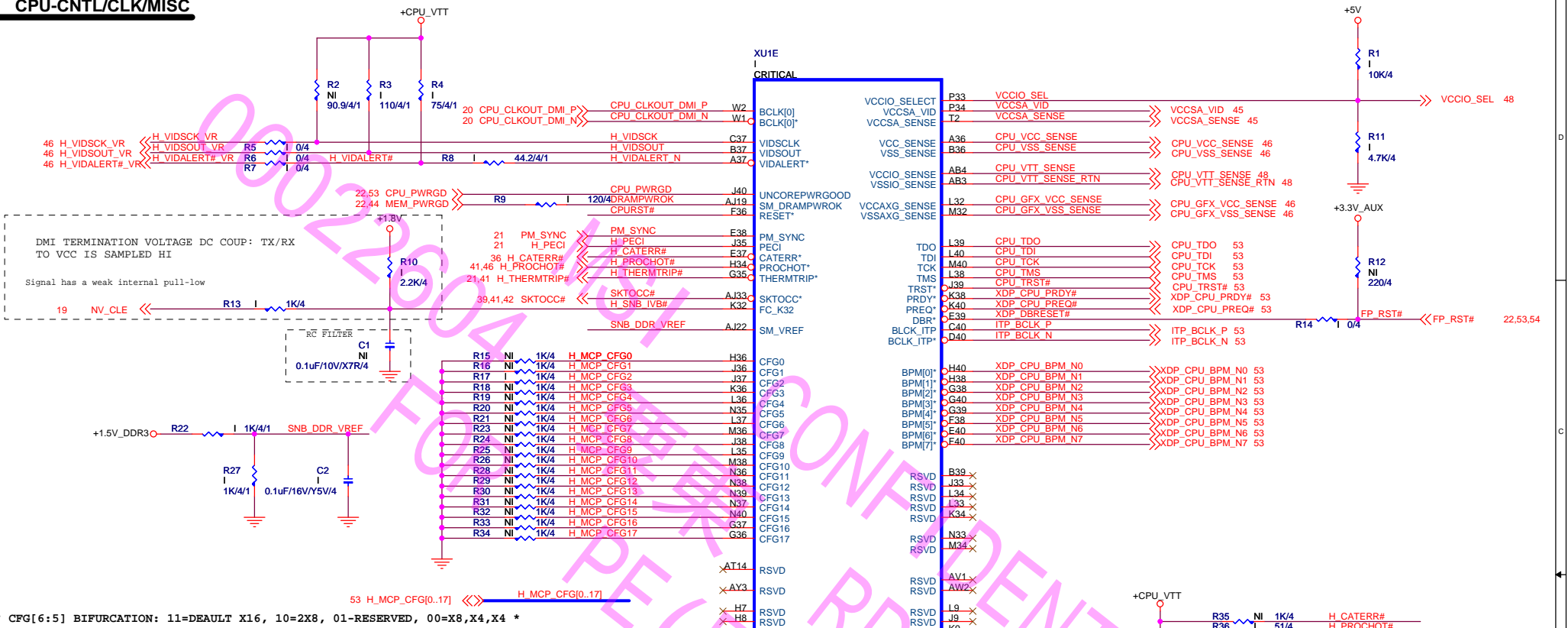


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CPU-CNTL/CLK/MISC



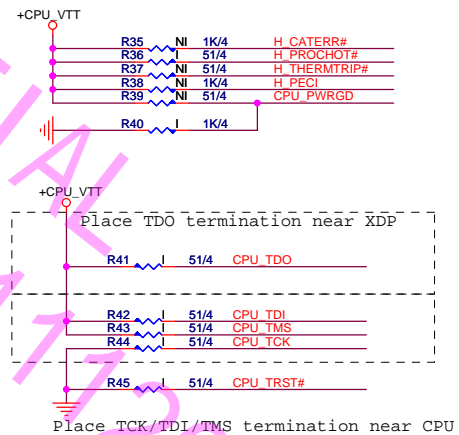
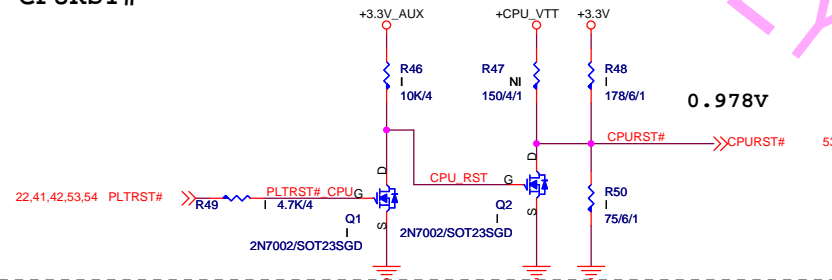
* CFG[6:5] BIFURCATION: 11=DEAULT X16, 10=2X8, 01-RESERVED, 00=X8,X4,X4 *

| CFG | H | L | DESCRIPTION |
|-----|----------|----------|--------------------------|
| 0 | REVERSED | REVERSED | REVERSED |
| 1 | REVERSED | REVERSED | REVERSED |
| 2 | NORM | REVERS | PEG LANE REVERSAL[0],X16 |
| 3 | REVERSED | REVERSED | REVERSED |
| 4 | REVERSED | REVERSED | REVERSED |
| 5 | * | * | PCIE BIFURCATION |
| 6 | * | * | PCIE BIFURCATION |
| 7 | REVERSED | REVERSED | REVERSED |
| 8 | REVERSED | REVERSED | REVERSED |
| 9 | REVERSED | REVERSED | REVERSED |
| 10 | REVERSED | REVERSED | REVERSED |
| 11 | REVERSED | REVERSED | REVERSED |
| 12 | REVERSED | REVERSED | REVERSED |
| 13 | REVERSED | REVERSED | REVERSED |
| 14 | REVERSED | REVERSED | REVERSED |
| 15 | REVERSED | REVERSED | REVERSED |

CFG 3,4,5,6,7,8,9 HAVE INTERNAL PULL-UPS

PEG CONFIG TABLE

| SEL2 | SEL1 | SEL0 | PCIE CONFIG |
|------|------|------|-------------|
| 1 | 1 | 1 | 1 X 16 |
| 1 | 1 | 0 | 2 X 8 |



Release Date : **Wednesday, November 23, 2011**

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HP SCH P/N: 675886-000 (MSI MS-7782)

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| Size | Custom |
|------|--------|

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Sheet 7 of 63

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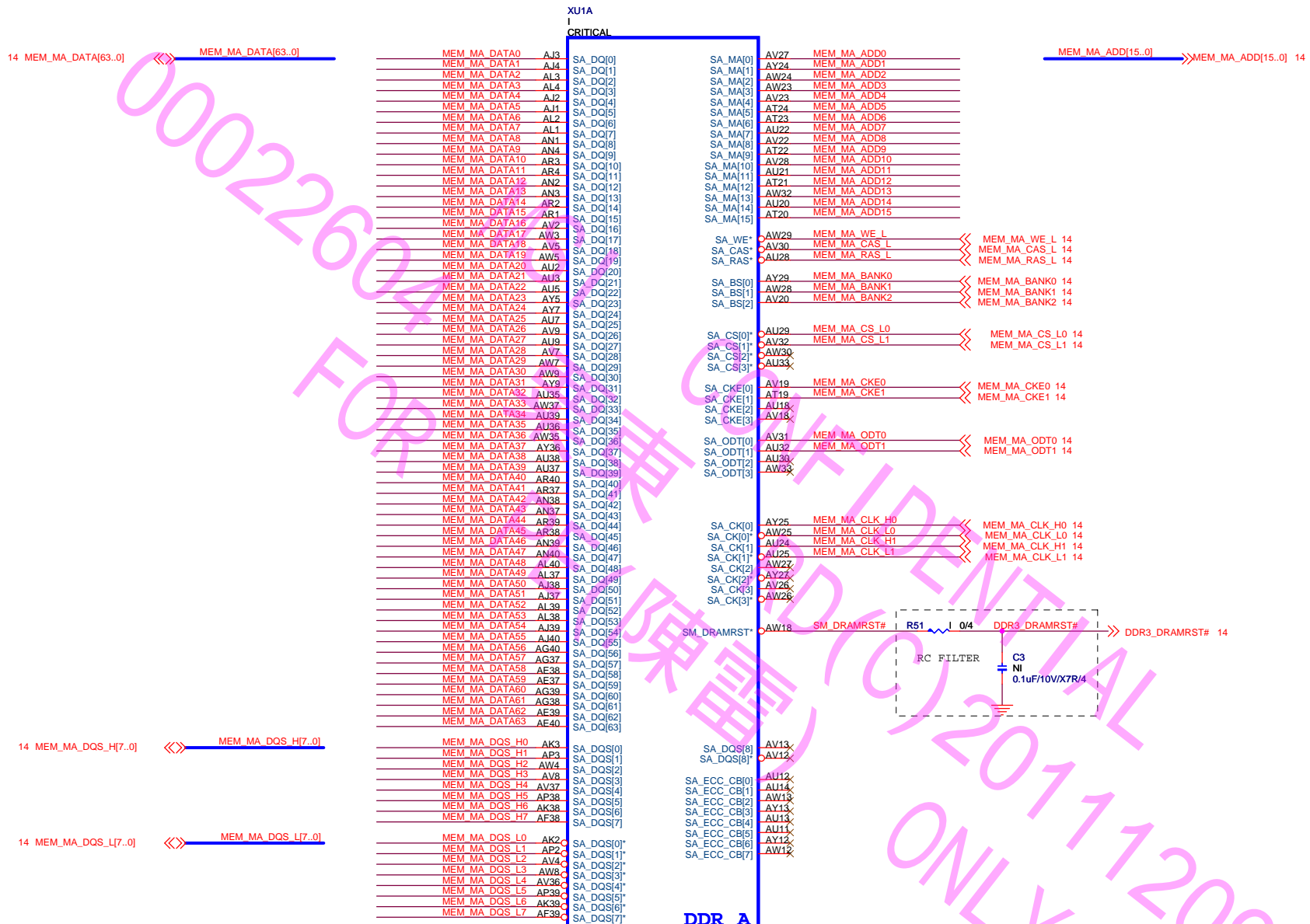
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

| | |
|--------|-----------------------|
| Size | Document Description |
| Custom | CPU-Memory-CHA |

Rev
X2

| | |
|-------|---------------|
| Date: | Sheet 8 of 63 |
|-------|---------------|



DDR A

1 OF 11

SOCKET H2

CPU Memory CH-B

15 MEM_MB_DATA[63..0] >>> MEM_MB_DATA[63..0]

DQ8-15 remapping implemented
to improve breakout and
minimize CH-2-CH couplingDQ49-56 remapping implemented
to improve breakout and
minimize CH-2-CH coupling

15 MEM_MB_DQS_H[7..0] <<< MEM_MB_DQS_H[7..0]

15 MEM_MB_DQS_L[7..0] <<< MEM_MB_DQS_L[7..0]

XU1B

CRITICAL

MEM_MB_DATA0 AG7
MEM_MB_DATA1 AG8
MEM_MB_DATA2 AJ8
MEM_MB_DATA3 AJ9
MEM_MB_DATA4 AG5
MEM_MB_DATA5 AG6
MEM_MB_DATA6 AJ6
MEM_MB_DATA7 AJ7
MEM_MB_DATA13 AL7
MEM_MB_DATA9 AM7
MEM_MB_DATA15 AL10
MEM_MB_DATA12 AL6
MEM_MB_DATA8 AM6
MEM_MB_DATA14 AL9
MEM_MB_DATA10 AM9
MEM_MB_DATA16 AP7
MEM_MB_DATA17 AR7
MEM_MB_DATA18 AP10
MEM_MB_DATA19 AR10
MEM_MB_DATA20 AP6
MEM_MB_DATA21 AR6
MEM_MB_DATA22 AP9
MEM_MB_DATA23 AR9
MEM_MB_DATA24 AM12
MEM_MB_DATA25 AM13
MEM_MB_DATA26 AR13
MEM_MB_DATA27 AP13
MEM_MB_DATA28 AL12
MEM_MB_DATA29 AL13
MEM_MB_DATA30 AR12
MEM_MB_DATA31 AP12
MEM_MB_DATA32 AR28
MEM_MB_DATA33 AR29
MEM_MB_DATA34 AL28
MEM_MB_DATA35 AL29
MEM_MB_DATA36 AP28
MEM_MB_DATA37 AP29
MEM_MB_DATA38 AM28
MEM_MB_DATA39 AM29
MEM_MB_DATA40 AP32
MEM_MB_DATA41 AP31
MEM_MB_DATA42 AP35
MEM_MB_DATA43 AP34
MEM_MB_DATA44 AR32
MEM_MB_DATA45 AR31
MEM_MB_DATA46 AR33
MEM_MB_DATA47 AR34
MEM_MB_DATA48 AM32
MEM_MB_DATA49 AM31
MEM_MB_DATA55 AL35
MEM_MB_DATA51 AL32
MEM_MB_DATA54 AM34
MEM_MB_DATA49 AL31
MEM_MB_DATA53 AM35
MEM_MB_DATA50 AL34
MEM_MB_DATA56 AH35
MEM_MB_DATA57 AH34
MEM_MB_DATA58 AE34
MEM_MB_DATA59 AE35
MEM_MB_DATA60 AJ35
MEM_MB_DATA61 AJ34
MEM_MB_DATA62 AE33
MEM_MB_DATA63 AE35

MEM_MB_DQS_H0 AH7
MEM_MB_DQS_H1 AM8
MEM_MB_DQS_H2 AR8
MEM_MB_DQS_H3 AN13
MEM_MB_DQS_H4 AN29
MEM_MB_DQS_H5 AP33
MEM_MB_DQS_H6 AL33
MEM_MB_DQS_H7 AG35

MEM_MB_DQS_L0 AH6
MEM_MB_DQS_L1 AL8
MEM_MB_DQS_L2 AP8
MEM_MB_DQS_L3 AN12
MEM_MB_DQS_L4 AN28
MEM_MB_DQS_L5 AR33
MEM_MB_DQS_L6 AM33
MEM_MB_DQS_L7 AG34

DDR_B

2 OF 11

SOCKET H2

SB_MA[0] AK24
SB_MA[1] AM20
SB_MA[2] AM19
SB_MA[3] AK18
SB_MA[4] AP19
SB_MA[5] AP18
SB_MA[6] AM18
SB_MA[7] AL18
SB_MA[8] AN18
SB_MA[9] AY17
SB_MA[10] AN23
SB_MA[11] AU17
SB_MA[12] AT18
SB_MA[13] AR26
SB_MA[14] AY16
SB_MA[15] AV16

MEM_MB_ADD0
MEM_MB_ADD1
MEM_MB_ADD2
MEM_MB_ADD3
MEM_MB_ADD4
MEM_MB_ADD5
MEM_MB_ADD6
MEM_MB_ADD7
MEM_MB_ADD8
MEM_MB_ADD9
MEM_MB_ADD10
MEM_MB_ADD11
MEM_MB_ADD12
MEM_MB_ADD13
MEM_MB_ADD14
MEM_MB_ADD15

MEM_MB_ADD[15..0] >>> MEM_MB_ADD[15..0] 15

SB_WE* AR25
SB_CAS* AK25
SB_RAS* AP24

MEM_MB_WE_L 15
MEM_MB_CAS_L 15
MEM_MB_RAS_L 15

SB_BS[0] AP23
SB_BS[1] AM24
SB_BS[2] AW17

MEM_MB_BANK0 15
MEM_MB_BANK1 15
MEM_MB_BANK2 15

SB_CS[0]* AN25
SB_CS[1]* AN26
SB_CS[2]* AL25
SB_CS[3]* AT26

MEM_MB_CS_L0 15
MEM_MB_CS_L1 15

SB_CKE[0] AL16
SB_CKE[1] AY15
SB_CKE[2] AW15
SB_CKE[3] AV15

MEM_MB_CKE0 15
MEM_MB_CKE1 15

SB_ODT[0] AL26
SB_ODT[1] AP26
SB_ODT[2] AM29
SB_ODT[3] AK29

MEM_MB_ODT0 15
MEM_MB_ODT1 15

SB_CK[0] AL21
SB_CK[0]* AL22
SB_CK[1] AL20
SB_CK[1]* AK20
SB_CK[2] AL23
SB_CK[2]* AM22
SB_CK[3] AP21
SB_CK[3]* AN21

MEM_MB_CLK_H0 15
MEM_MB_CLK_L0 15
MEM_MB_CLK_H1 15
MEM_MB_CLK_L1 15

FC_AH1 AH1
FC_AH4 AH4

MEM_MB_CPU_VREFDQ
MEM_MA_CPU_VREFDQ

MEM_MB_CPU_VREFDQ 16
MEM_MA_CPU_VREFDQ 16

C4
0.1uF/16V/Y5V/4

C5
0.1uF/16V/Y5V/4

SB_DQS[8] AN18
SB_DQS[8]* AN19

SB_ECC_CB[0] AL16
SB_ECC_CB[1] AM16
SB_ECC_CB[2] AP16
SB_ECC_CB[3] AR16
SB_ECC_CB[4] AL15
SB_ECC_CB[5] AM15
SB_ECC_CB[6] AS15
SB_ECC_CB[7] AP19

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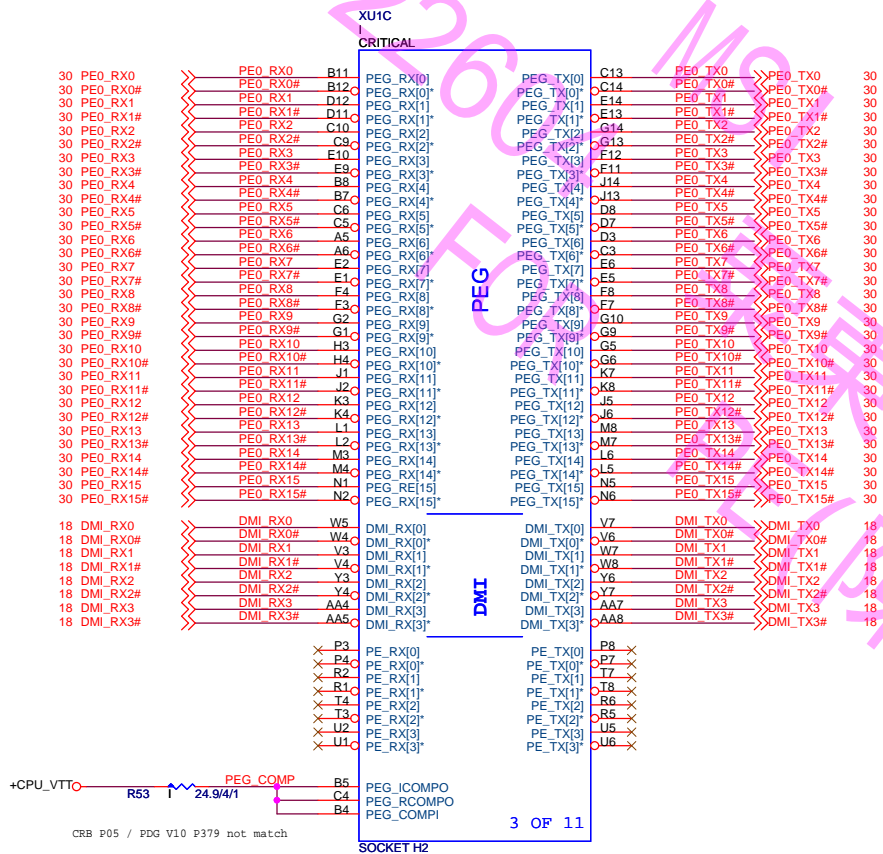


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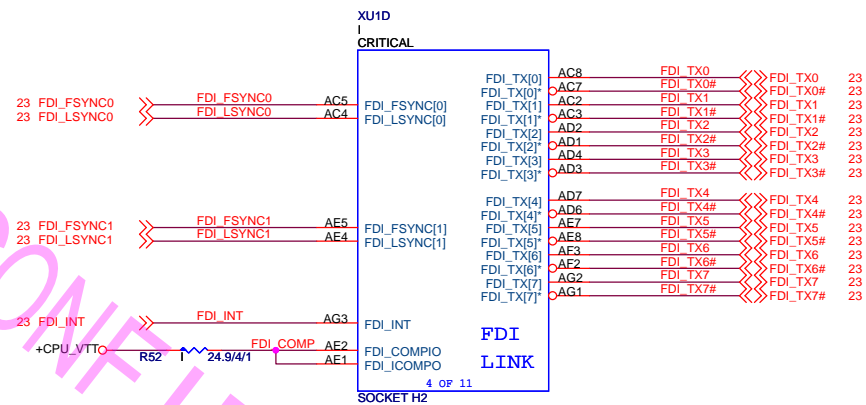
HP SCH P/N: 675886-000 (MSI MS-7782)

| Size Custom | Document Description | Rev X2 |
|-------------|----------------------|--------|
| | CPU-Memory-CHB | |
| Date: | Sheet 9 of 63 | |

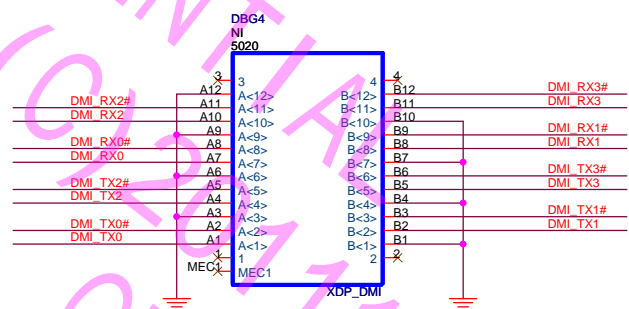
CPU-PCIE / DMI



CPU-FDI



XDP-DMI



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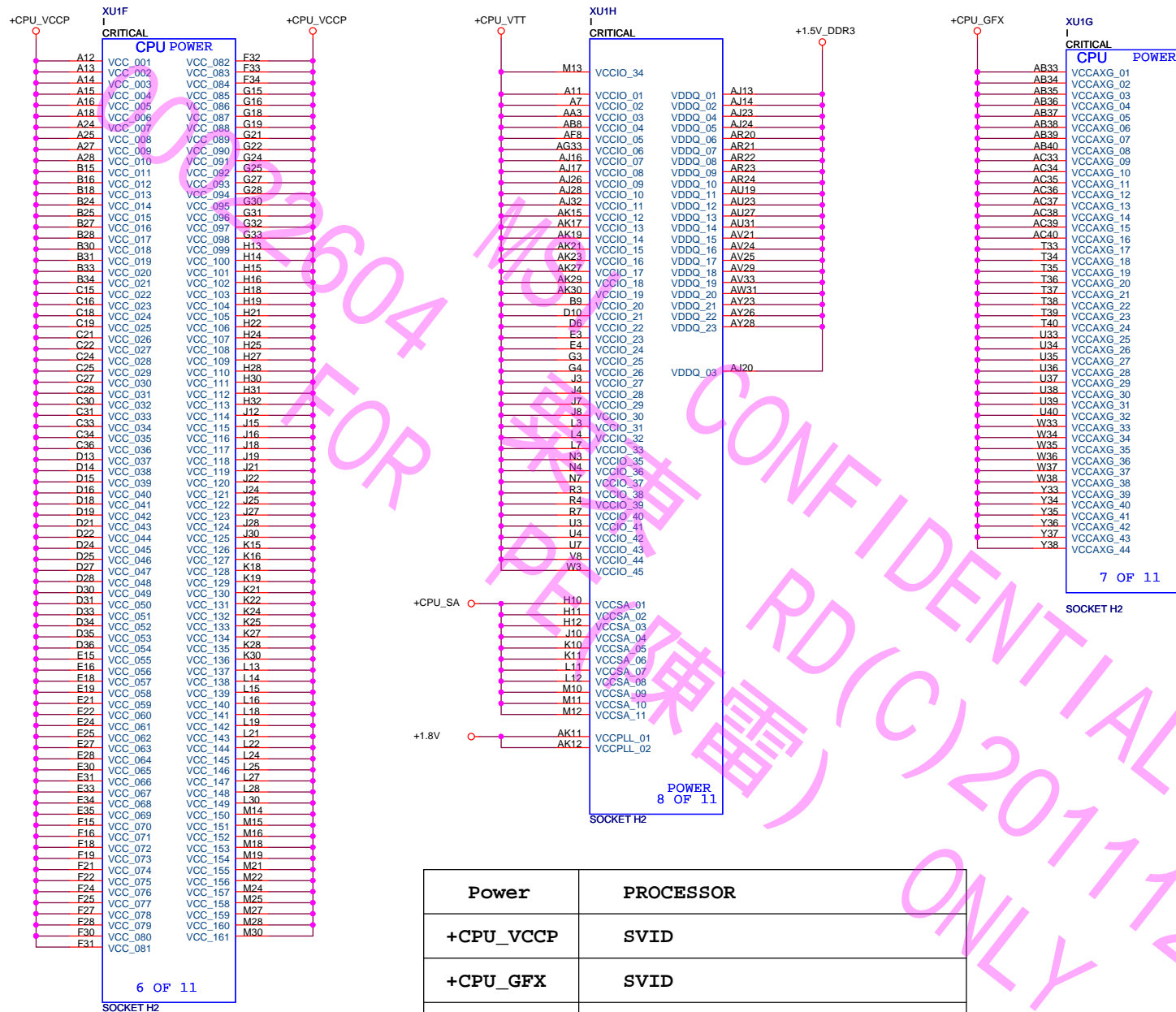


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| | | |
|----------------|---|-----------|
| Size Custom | Document Description CPU-PCIE/DMI | Rev X2 |
| Date: | Sheet | 10 of 63 |

CPU-POWER



| Power | PROCESSOR |
|------------|-------------|
| +CPU_VCCP | SVID |
| +CPU_GFX | SVID |
| +CPU_VTT | 1.05V/1.00V |
| +CPU_SA | 0.96V/0.85V |
| +1.5V_DDR3 | 1.5V |
| +1.8V | 1.8V |

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|--------------------------------------|----------------------|--------|
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| Size Custom | Document Description | Rev X2 |
| CPU-Power | | |
| Date: | Sheet 11 of 63 | |

CPU-GND

XU1I

CRITICAL

A17 VSS_001 VSS_091 AM27
A23 VSS_002 VSS_092 AM3
A26 VSS_003 VSS_093 AM30
A29 VSS_004 VSS_094 AM36
A35 VSS_005 VSS_095 AM37
AA33 VSS_006 VSS_096 AM38
AA34 VSS_007 VSS_097 AM39
AA35 VSS_008 VSS_098 AM4
AA36 VSS_009 VSS_099 AM40
AA37 VSS_010 VSS_100 AM5
AA38 VSS_011 VSS_101 AN10
AA6 VSS_012 VSS_102 AN11
AB5 VSS_013 VSS_103 AN14
AC1 VSS_014 VSS_104 AN17
AC6 VSS_015 VSS_105 AN19
AD33 VSS_016 VSS_106 AN22
AD36 VSS_017 VSS_107 AN24
AD38 VSS_018 VSS_108 AN27
AD39 VSS_019 VSS_109 AN30
AD40 VSS_020 VSS_110 AN31
AD5 VSS_021 VSS_111 AN32
AD8 VSS_022 VSS_112 AN33
AE3 VSS_023 VSS_113 AN34
AE33 VSS_024 VSS_114 AN35
AE36 VSS_025 VSS_115 AN36
AF1 VSS_026 VSS_116 AN5
AF34 VSS_027 VSS_117 AN6
AF36 VSS_028 VSS_118 AN7
AF37 VSS_029 VSS_119 AN8
AF40 VSS_030 VSS_120 AN9
AF5 VSS_031 VSS_121 AP1
AF6 VSS_032 VSS_122 AP11
AF7 VSS_033 VSS_123 AP14
AG36 VSS_034 VSS_124 AP17
AH2 VSS_035 VSS_125 AP22
AH3 VSS_036 VSS_126 AP25
AH33 VSS_037 VSS_127 AP27
AH36 VSS_038 VSS_128 AP30
AH37 VSS_039 VSS_129 AP36
AH38 VSS_040 VSS_130 AP37
AH39 VSS_041 VSS_131 AP4
AH40 VSS_042 VSS_132 AP40
AH5 VSS_043 VSS_133 AP5
AH8 VSS_044 VSS_134 AR11
AJ12 VSS_045 VSS_135 AR14
AJ15 VSS_046 VSS_136 AR17
AJ18 VSS_047 VSS_137 AR18
AJ21 VSS_048 VSS_138 AR19
AJ25 VSS_049 VSS_139 AR27
AJ27 VSS_050 VSS_140 AR30
AJ38 VSS_051 VSS_141 AR37
AJ5 VSS_052 VSS_142 AR5
AK1 VSS_053 VSS_143 AT1
AK10 VSS_054 VSS_144 AT10
AK13 VSS_055 VSS_145 AT12
AK14 VSS_056 VSS_146 AT13
AK16 VSS_057 VSS_147 AT15
AK22 VSS_058 VSS_148 AT16
AK28 VSS_059 VSS_149 AT17
AK31 VSS_060 VSS_150 AT2
AK32 VSS_061 VSS_151 AT25
AK33 VSS_062 VSS_152 AT27
AK34 VSS_063 VSS_153 AT28
AK35 VSS_064 VSS_154 AT29
AK36 VSS_065 VSS_155 AT3
AK37 VSS_066 VSS_156 AT30
AK4 VSS_067 VSS_157 AT31
AK40 VSS_068 VSS_158 AT32
AK5 VSS_069 VSS_159 AT33
AK6 VSS_070 VSS_160 AT34
AK7 VSS_071 VSS_161 AT35
AK8 VSS_072 VSS_162 AT36
AK9 VSS_073 VSS_163 AT37
AL11 VSS_074 VSS_164 AT38
AL14 VSS_075 VSS_165 AT39
AL17 VSS_076 VSS_166 AT4
AL19 VSS_077 VSS_167 AT40
AL24 VSS_078 VSS_168 AT5
AL27 VSS_079 VSS_169 AT6
AL30 VSS_080 VSS_170 AT7
AL36 VSS_081 VSS_171 AT8
AL5 VSS_082 VSS_172 AT9
AM1 VSS_083 VSS_173 AU1
AM11 VSS_084 VSS_174 AU15
AM14 VSS_085 VSS_175 AU26
AM17 VSS_086 VSS_176 AU34
AM2 VSS_087 VSS_177 AU4
AM21 VSS_088 VSS_178 AU6
AM23 VSS_089 VSS_179 AU8
AM25 VSS_090 VSS_180 AV10
A4 VSS_VCTF_01
AV39 VSS_VCTF_02

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SOCKET H2

XU1J

CRITICAL

AV11 VSS_181 VSS_271 G8
AV14 VSS_182 VSS_272 H1
AV17 VSS_183 VSS_273 H17
AV3 VSS_184 VSS_274 H2
AV35 VSS_185 VSS_275 H20
AV38 VSS_186 VSS_276 H23
AV8 VSS_187 VSS_277 H26
AW10 VSS_188 VSS_278 H29
AW11 VSS_189 VSS_279 H33
AW14 VSS_190 VSS_280 H35
AW16 VSS_191 VSS_281 H37
AW36 VSS_192 VSS_282 H39
AW6 VSS_193 VSS_283 H5
AY11 VSS_194 VSS_284 H6
AY14 VSS_195 VSS_285 H9
AY18 VSS_196 VSS_286 H11
AY35 VSS_197 VSS_287 H17
AY4 VSS_198 VSS_288 J20
AY6 VSS_199 VSS_289 J23
AY8 VSS_200 VSS_290 J26
B10 VSS_201 VSS_291 J29
B13 VSS_202 VSS_292 J32
B14 VSS_203 VSS_293 K1
B17 VSS_204 VSS_294 K12
B23 VSS_205 VSS_295 K13
B26 VSS_206 VSS_296 K14
B29 VSS_207 VSS_297 K17
B32 VSS_208 VSS_298 K2
B35 VSS_209 VSS_299 K29
B38 VSS_210 VSS_300 K26
B6 VSS_211 VSS_301 K29
C11 VSS_212 VSS_302 K33
C12 VSS_213 VSS_303 K33
C17 VSS_214 VSS_304 K35
C20 VSS_215 VSS_305 K37
C23 VSS_216 VSS_306 K39
C26 VSS_217 VSS_307 K5
C29 VSS_218 VSS_308 K6
C32 VSS_219 VSS_309 L10
C35 VSS_220 VSS_310 L17
C7 VSS_221 VSS_311 L20
C8 VSS_222 VSS_312 L23
D17 VSS_223 VSS_313 L26
D2 VSS_224 VSS_314 L29
D20 VSS_225 VSS_315 L8
D23 VSS_226 VSS_316 M1
D26 VSS_227 VSS_317 M17
D29 VSS_228 VSS_318 M2
D32 VSS_229 VSS_319 M20
D37 VSS_230 VSS_320 M23
D39 VSS_231 VSS_321 M26
D5 VSS_232 VSS_322 M29
D9 VSS_233 VSS_323 M33
E11 VSS_234 VSS_324 M35
E12 VSS_235 VSS_325 M37
E17 VSS_236 VSS_326 M39
E20 VSS_237 VSS_327 M5
E23 VSS_238 VSS_328 M6
E26 VSS_239 VSS_329 M9
E29 VSS_240 VSS_330 M8
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E7 VSS_243 VSS_333 P36
E8 VSS_244 VSS_334 P38
E9 VSS_245 VSS_335 P40
F1 VSS_246 VSS_336 P5
F10 VSS_247 VSS_337 P6
F13 VSS_248 VSS_338 R33
F14 VSS_249 VSS_339 R35
F17 VSS_250 VSS_340 R37
F2 VSS_251 VSS_341 R39
F20 VSS_252 VSS_342 R8
F23 VSS_253 VSS_343 T1
F26 VSS_254 VSS_344 T5
F29 VSS_255 VSS_345 T6
F35 VSS_256 VSS_346 T8
F37 VSS_257 VSS_347 V1
F39 VSS_258 VSS_348 V2
F5 VSS_259 VSS_349 V33
F6 VSS_260 VSS_350 V34
F9 VSS_261 VSS_351 V35
G11 VSS_262 VSS_352 V36
G12 VSS_263 VSS_353 V37
G17 VSS_264 VSS_354 V38
G20 VSS_265 VSS_355 V39
G23 VSS_266 VSS_356 V40
G26 VSS_267 VSS_357 V5
G29 VSS_268 VSS_358 W6
G34 VSS_269 VSS_359 W5
G7 VSS_270 VSS_360 Y8
AY37 VSS_NVTF_03
B3 VSS_NVTF_04

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SOCKET H2

XU1K

CRITICAL

BALLAMP_REV=1.4
AB7 RSVD_04
AD37 RSVD_05
AG4 RSVD_08
AJ29 RSVD_10
AJ30 RSVD_11
AJ31 RSVD_12
AJ34 RSVD_19
AW34 RSVD_21
P35 RSVD_43
P37 RSVD_44
P39 RSVD_45
R34 RSVD_46
R38 RSVD_47
R38 RSVD_48
R40 RSVD_49
RSVD_15
RSVD_14
RSVD_13
RSVD_17
RSVD_22
RSVD_07
RSVD_03
RSVD_06
RSVD_09
RSVD_27
RSVD_26
RSVD_25
RSVD_31
RSVD_41
D38
C39
C38
J34
N34
TP CPU C38 NOBOM
TP CPU N34 NOBOM

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SOCKET H2

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Size

Custom

Document Description

CPU-GND

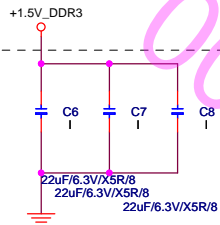
Rev

X2

Date:

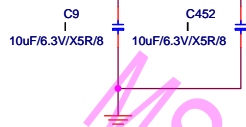
Sheet 12 of 63

+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS 22uF X3

+CPU_SA

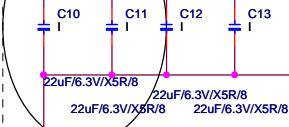


BOTTOM SIDE 22uF X 2

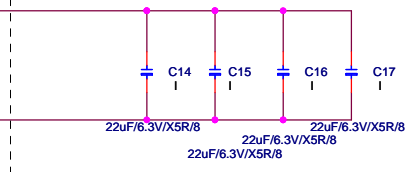
+CPU_GFX Decoupling

+CPU_GFX

SI:780343



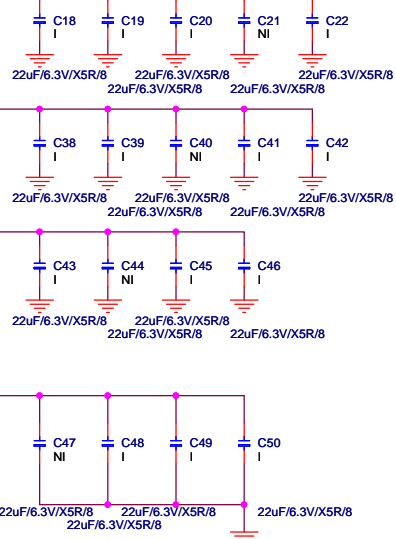
BOTTOM SIDE 22uF X 4



CPU SOCKET CAVITY CAPS 22uF X 4

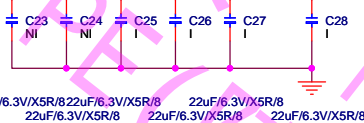
+CPU_VCCP-Decoupling

+CPU_VCCP



INSIDE CPU SOCKET CAVITY 22uF X 14

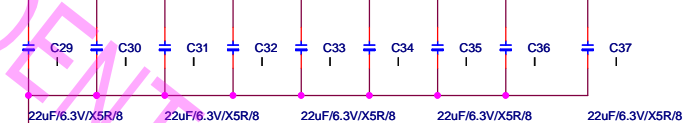
+CPU_VCCP



BOTTOM SIDE 22uF X 4

+CPU_VTT Decoupling

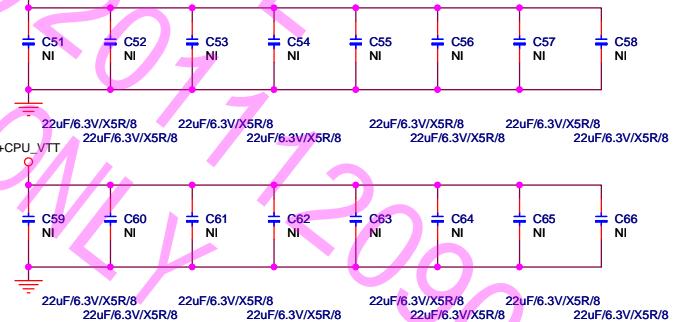
+CPU_VTT



CPU SOCKET CAVITY CAPS 22uF X 9

+CPU_VTT

BOTTOM SIDE 22uF X 0



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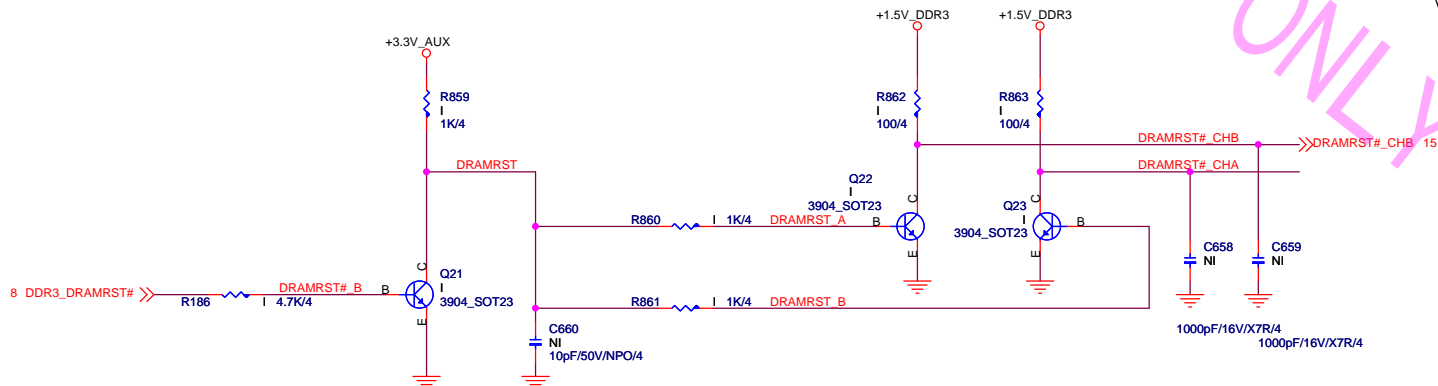
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| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description | Rev X2 |
| CPU-Decoupling | | |
| Date: | Sheet 13 | of 63 |

DDRIII CH-A DIMM1



ADDRESS: 1010 000

DDRIII-240P_BLACK-HF-1 **N13-2401081-L06**
BLACK COLOR



Release Date : Wednesday, November 23, 2011

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MICRO-STAR INT'L CO.,LTD

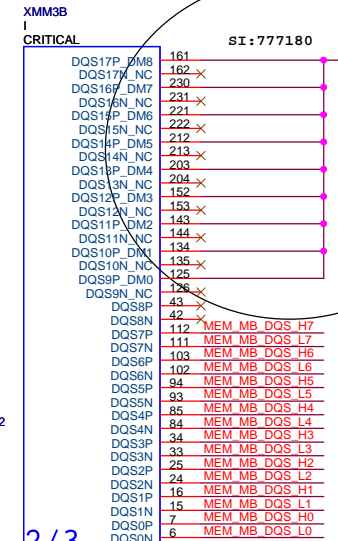
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DDR DIMM 1

| | |
|--|-----------|
| | Rev X2 |
|--|-----------|

MEM_MB_ADD[15..0] << MEM_MB_ADD[15..0] 9

MEM_MB_DATA[63..0] << MEM_MB_DATA[63..0] 9



ADDRESS: 1010 010

Black COLOR

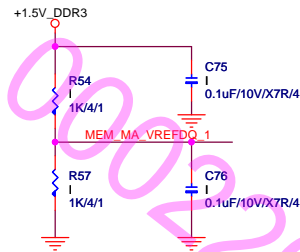
HP Restricted Secret



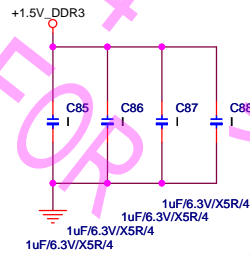
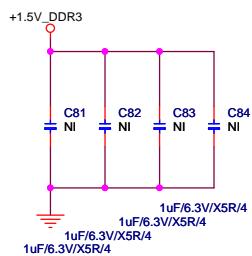
HP SCH P/N: 675886-000 (MSI MS-7782)

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|----------------|---|-----------|
| Size Custom | Document Description DDR DIMM 2 | Rev X2 |
| Date: | Sheet 15 of 63 | |

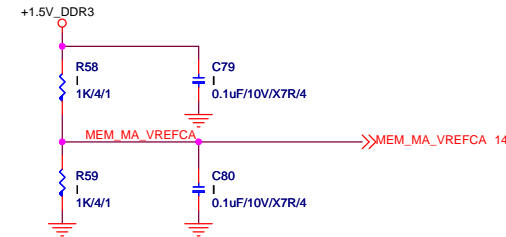
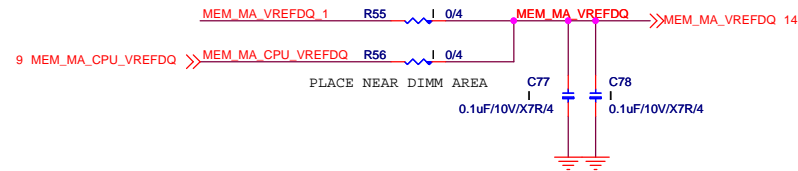
CHA



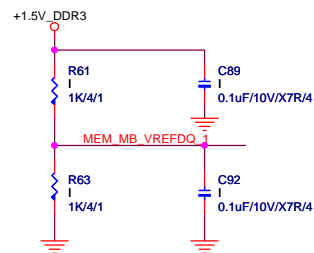
PLACE RESISTORS CLOSE TO CH_A DIMMS ON MEM_MA_VREFDQ



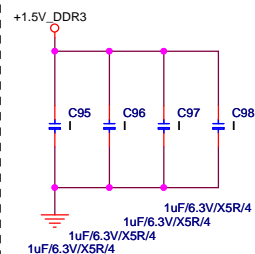
FOR XMM1



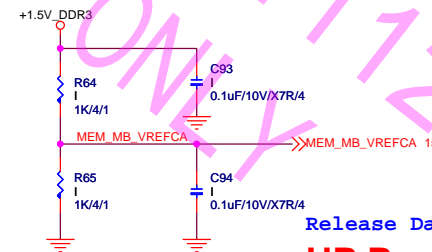
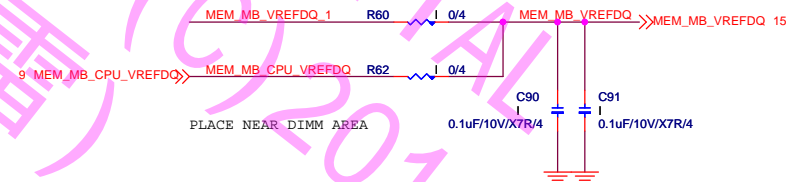
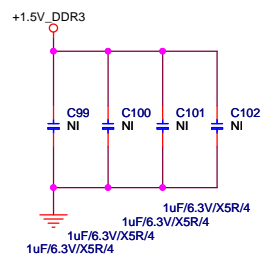
CHB



PLACE RESISTORS CLOSE TO CH_B DIMMS ON MEM_MB_VREFDQ



FOR XMM3



Release Date : Wednesday, November 23, 2011


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| | | |
|--------------------------------------|---|-----------|
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| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description CHA VREF OPTION | Rev X2 |
| Date: | Sheet 16 of 63 | |

00022604 MSI
FOR 栗東 CONFIDENTIAL
PE (陳雷) RD (C) 20111209007
ONLY

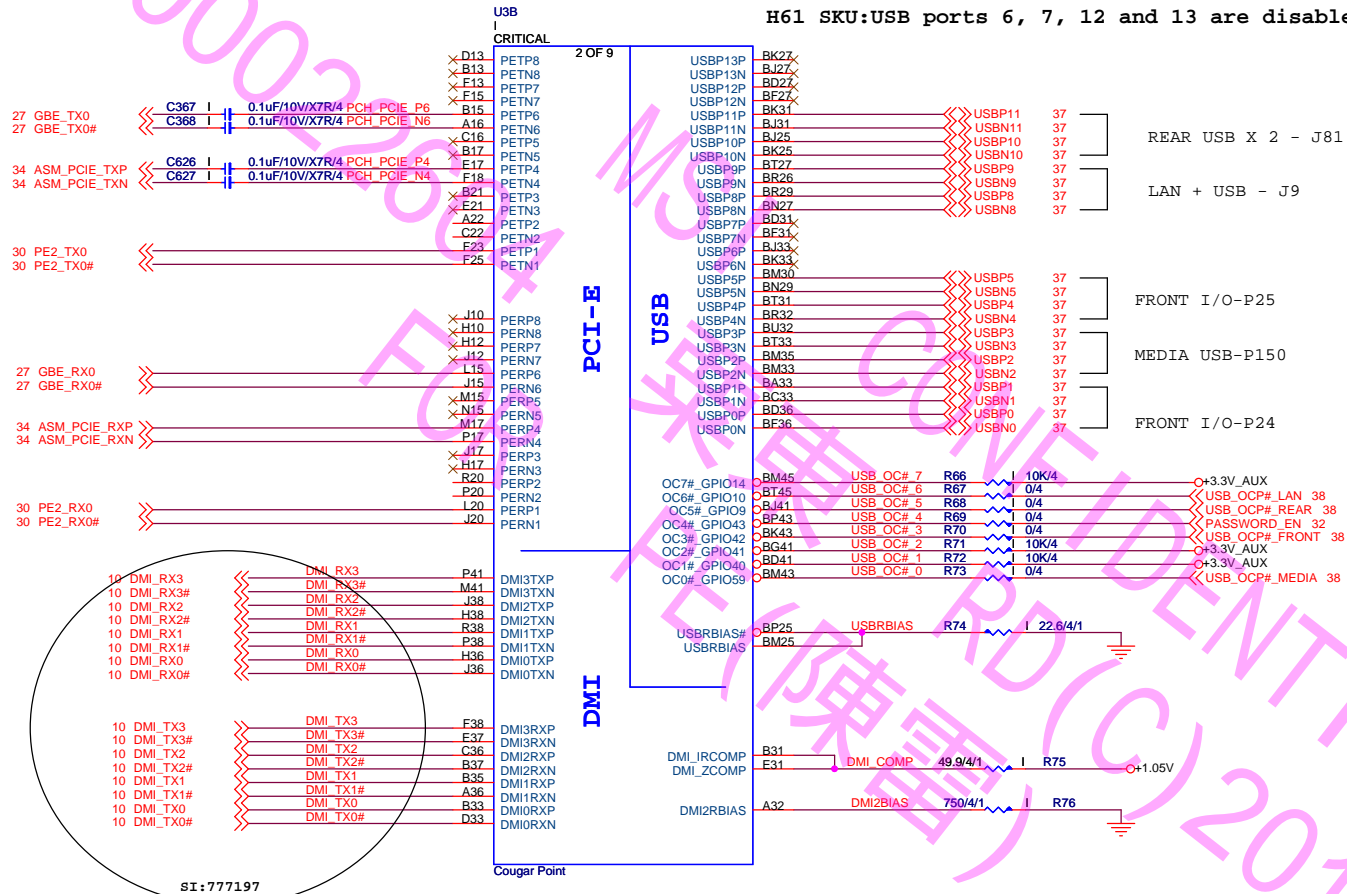
Release Date : Wednesday, November 23, 2011

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| | | | |
|---|--------------------------------------|---|-----------|
|  | MICRO-STAR INT'L CO.,LTD | | |
| | HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| | Size Custom | Document Description CHB VREF OPTION | Rev X2 |
| Date: | | Sheet 17 of 63 | |

PCH PCIE/DMI/USB

H61 SKU:PCie ports 7 and 8 are disabled.
H61 SKU:USB ports 6, 7, 12 and 13 are disabled.



| | | | | | |
|-----------|------|------------|-----------|-----------|----|
| USB OC# 7 | R219 | PROTO 33/4 | PCH XDP 7 | PCH_XDP_7 | 54 |
| USB OC# 6 | R352 | PROTO 33/4 | PCH XDP 6 | PCH_XDP_6 | 54 |
| USB OC# 5 | R442 | PROTO 33/4 | PCH XDP 5 | PCH_XDP_5 | 54 |
| USB OC# 4 | R444 | PROTO 33/4 | PCH XDP 4 | PCH_XDP_4 | 54 |
| USB OC# 3 | R457 | PROTO 33/4 | PCH XDP 3 | PCH_XDP_3 | 54 |
| USB OC# 2 | R791 | PROTO 33/4 | PCH XDP 2 | PCH_XDP_2 | 54 |
| USB OC# 1 | R792 | PROTO 33/4 | PCH XDP 1 | PCH_XDP_1 | 54 |
| USB OC# 0 | R793 | PROTO 33/4 | PCH XDP 0 | PCH_XDP_0 | 54 |

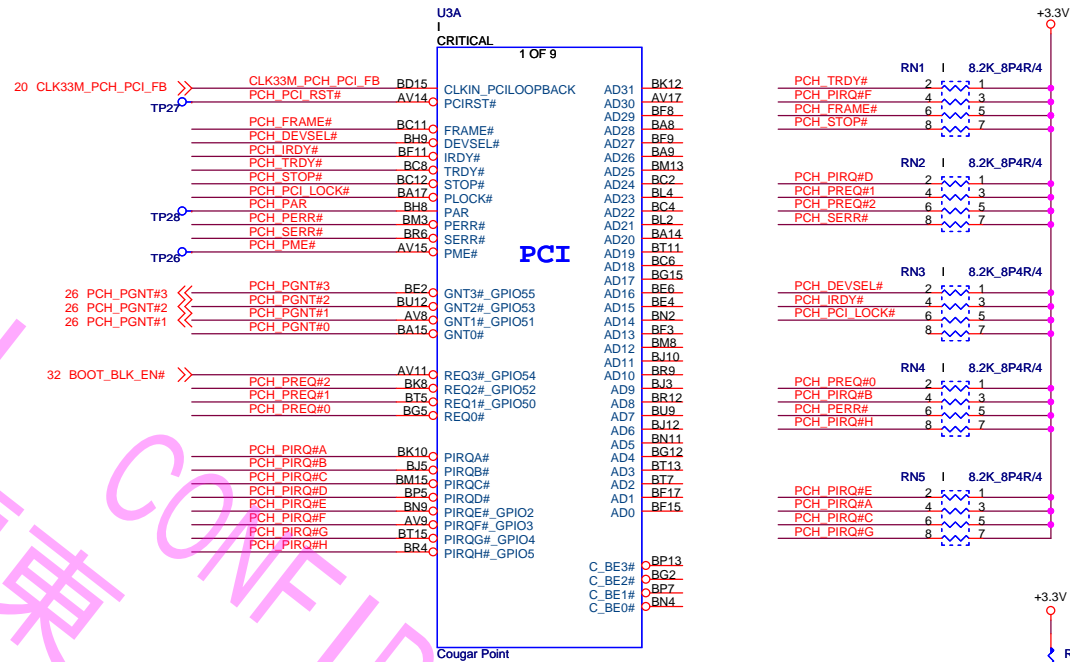
Release Date : Wednesday, November 23, 2011

HP Restricted Secret

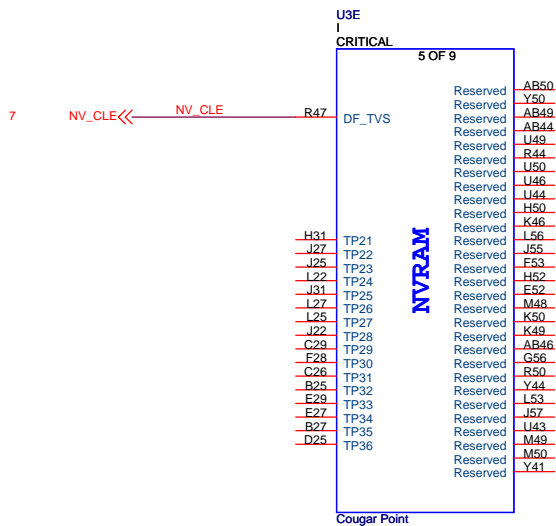
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| MICRO-STAR INT'L CO.,LTD | | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | | |
| Size Custom | Document Description | Rev X2 | |
| PCH PCIE/DMI/USB | | | |
| Date: | Sheet 18 of 63 | | |

00022604 MSI 00022604 FOR PE (陳雷) RD (C) 20111209 ONLY

PCH PCI



PCH NVRAM



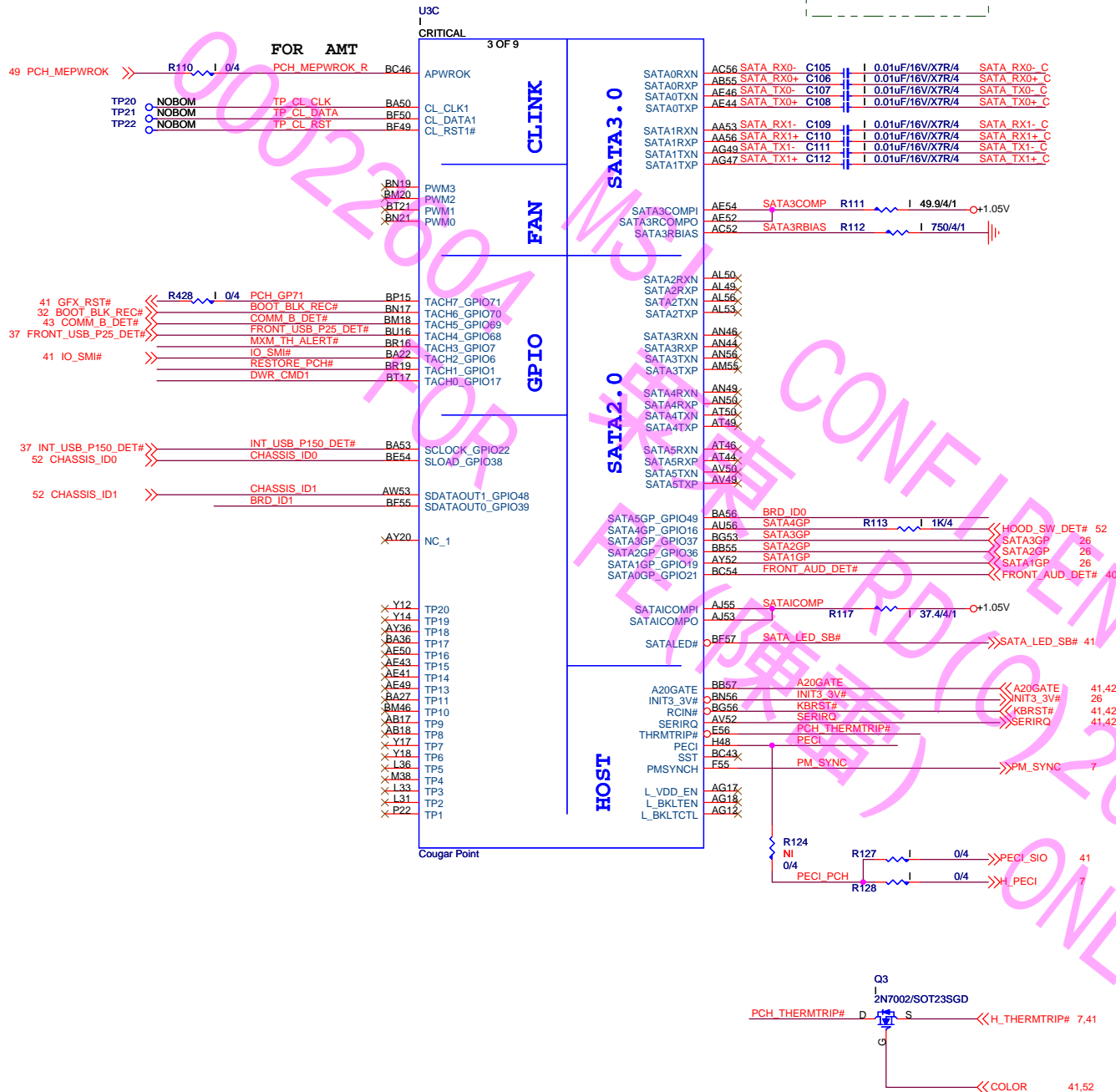
Release Date : Wednesday, November 23, 2011

HP Restricted Secret

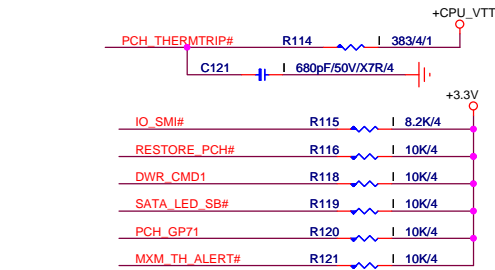
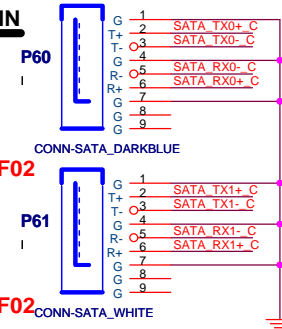
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|--------------------------------------|---------------------------------------|-------|-----------|
| MICRO-STAR INT'L CO.,LTD | | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | | |
| Size Custom | Document Description PCH PCI/NVRAM | | Rev X2 |
| | | | |
| Date: | | Sheet | 19 of 63 |

PCH SATAII/HOST/FAN/GPIO

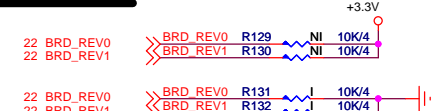
PLACE SATA AC COUPLING CAPS CLOSE TO U3



SATA II CONN



BOARD REV



PCA REVISION ID

| BOARD REV[1:0] | Enterprise Desktop |
|----------------|--------------------|
| 00 | All EVT |
| 01 | All DVT |
| 10 | PVT1 |
| 11 | PVT2+ |
| 00 | MVB, A |
| 01 | 1st Major ECN |
| 10 | 2nd Major ECN |
| 11 | 3rd Major ECN |

BOARD ID



PCA BOARD ID[2:0]

| Form Factor | Default | Commanders |
|-------------------|---------|------------|
| Small Form Factor | 011 | - |

Release Date : Wednesday, November 23, 2011

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MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

| Size | Document Description | Rev |
|--------|--------------------------|-----|
| Custom | PCH SATAII/HOST/FAN/GPIO | X2 |

Date: Sheet 21 of 63

PCH SMBUS/LPC/AUDIO/RTC

U3D

CRITICAL

4 OF 9

LPC

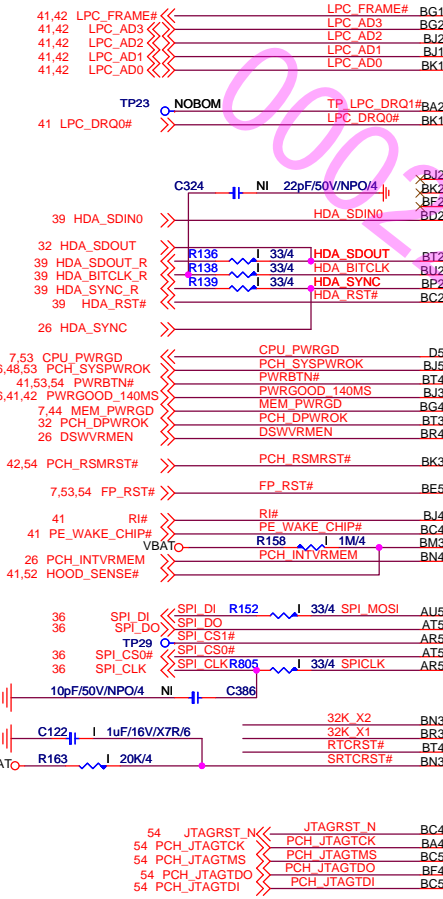
AUDIO

SPI

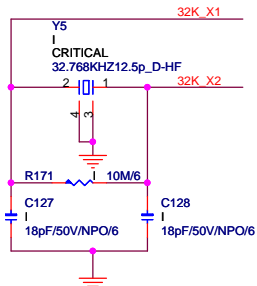
RTC

JTAG (SUS)

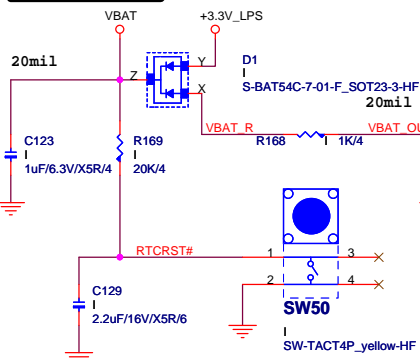
Cougar Point



32.768KHZ

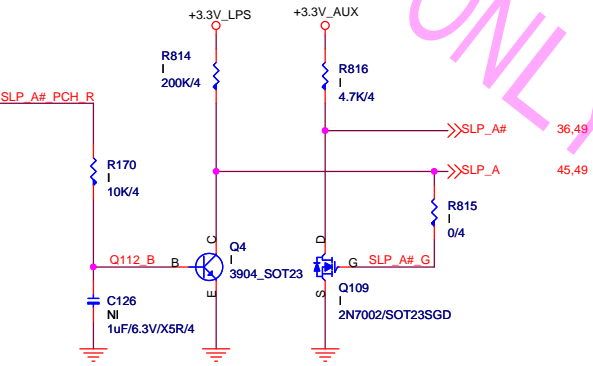


CLEAR CMOS

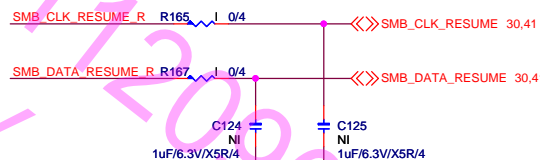


| | |
|------|------------------------|
| SW50 | SLIDE SWITCH OPERATION |
| | NORMAL OPERATION |
| | CLEAR CMOS |

SLP A



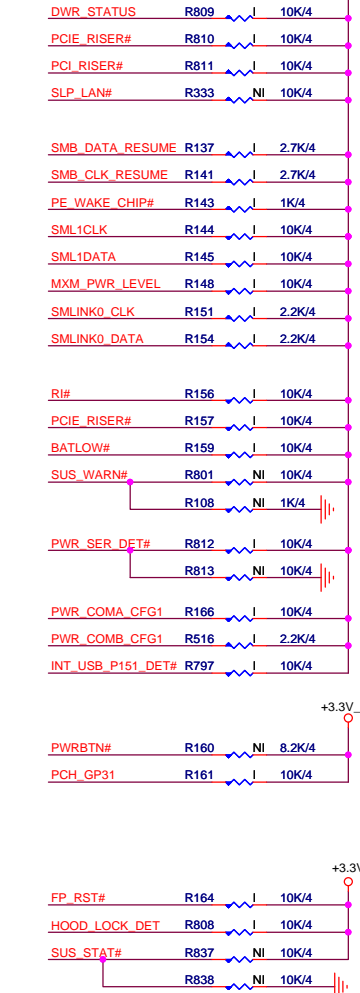
PLACE 0 OHM CLOS TO PCH



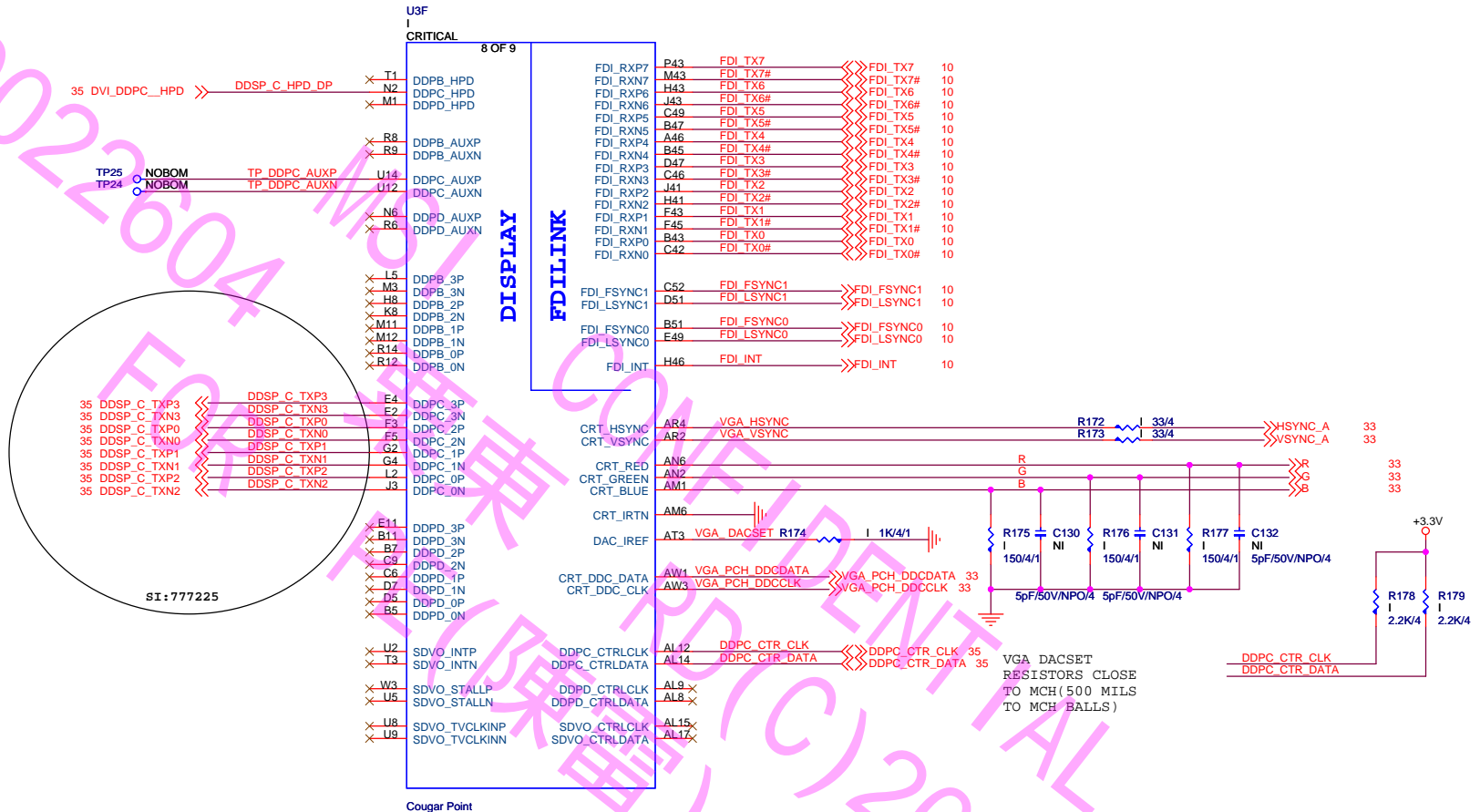
Release Date : Wednesday, November 23, 2011
HP Restricted Secret

| | | |
|--------------------------------------|----------------------|--------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description | Rev X2 |
| PCH SMBUS/LPC/AUDIO/RTC | | |
| Date: | Sheet 22 | of 63 |

PULL UP



PCH FDI/VGA/DP

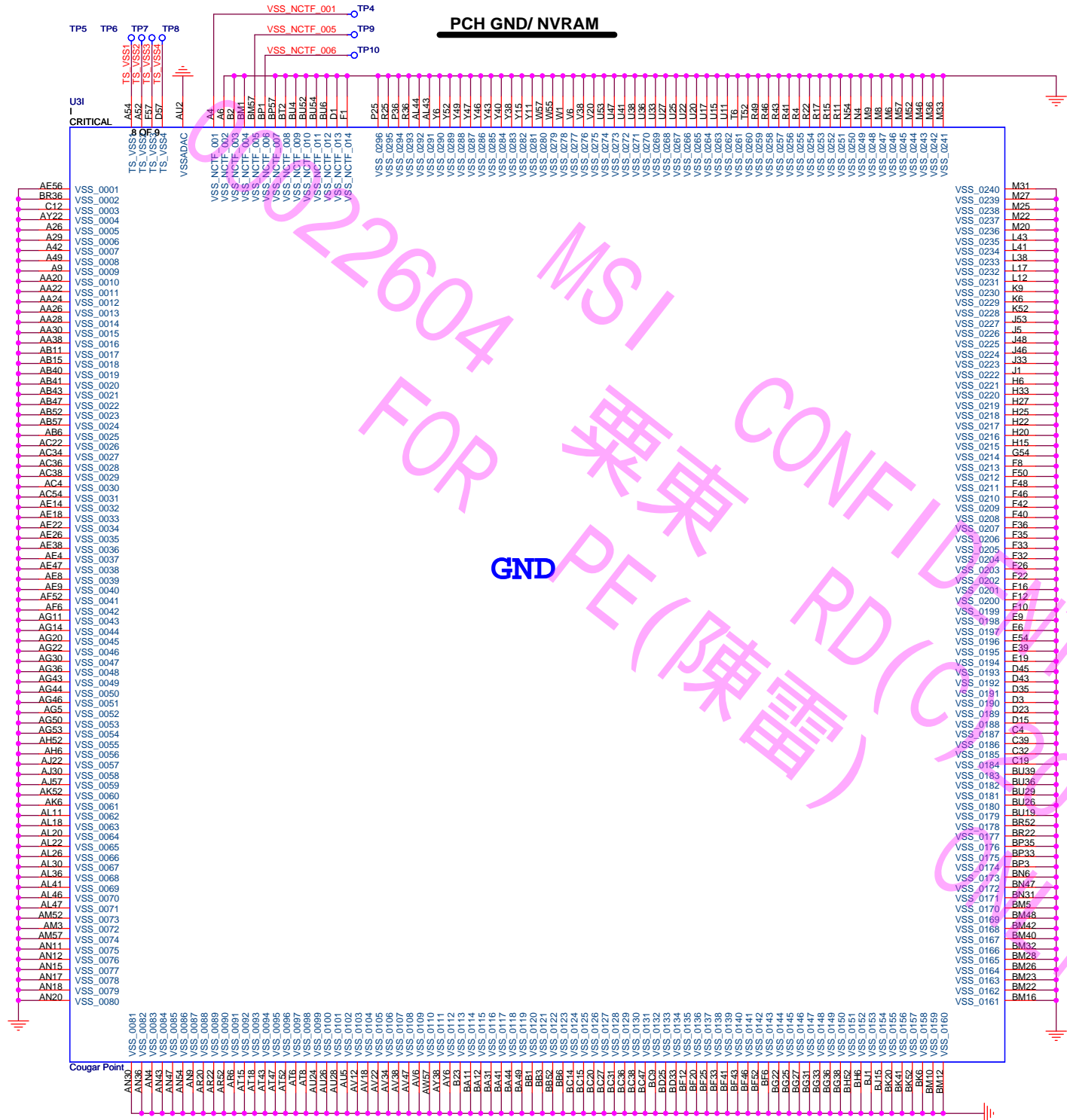


Release Date : Wednesday, November 23, 2011

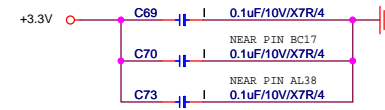
HP Restricted Secret

| | | |
|--------------------------------------|---|-----------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description PCH FDI/VGA/HDMI/DP/SDV | Rev X2 |
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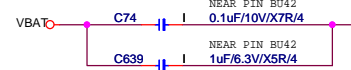
PCH GND/ NVRAM



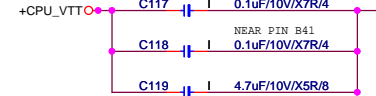
PCI/GPIO/LPC



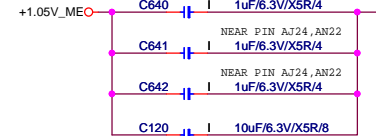
VCCRTC



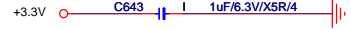
CPU



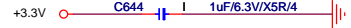
CORE



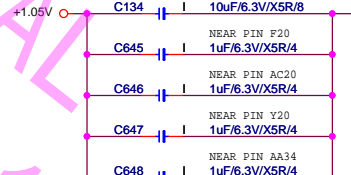
CLOCK GEN



HVCOMS



PCIE/DMI/FDI



PCIE/DMI



Release Date : Wednesday, November 23, 2011

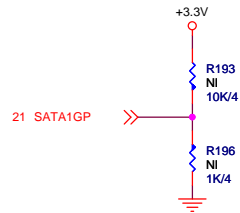
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|--------------------------------------|----------------------|--------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description | Rev X2 |
| PCH GND | | |
| Date: | Sheet 25 of 63 | |



REQUIRED STRAPS

| BOOT DEVICE | GNT1 | SATA1GP/GPIO19 |
|-------------|----------|----------------|
| LPC | 0 | 0 |
| PCI | 0 | Floating |
| SPI | Floating | Floating |



19 PCH_PGNT#1

INTVRMEN
0 : DISABLE INTERNAL VRM
1 : ENABLE INTERNAL VRM *

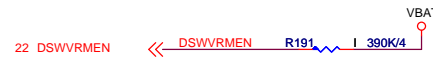
When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some events occur.
0: Can not to reset the processor.

DMI AC/DC MODE
0 : AC
1 : DC *

Topblock swap override when pull-low
Signal has a weak internal pull-up

GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

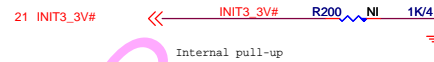
This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.



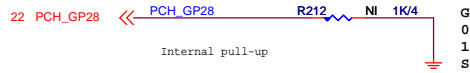
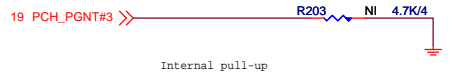
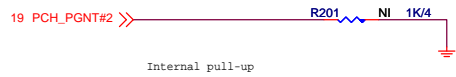
HDA_SYNC
OD PLL VR SUPPLY SEL
0 : 1.8V SUPPLY *
1 : 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



INT3_3V#
0 : ??????????????
1 : ?????????????? *



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up(8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high

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| | | |
|-------------|------------------------------------|--------|
| Size Custom | Document Description PCH STRAPS | Rev X2 |
| Date: | Sheet 26 of 63 | |

BCM 57788

P/N: B06-577880C-BX1

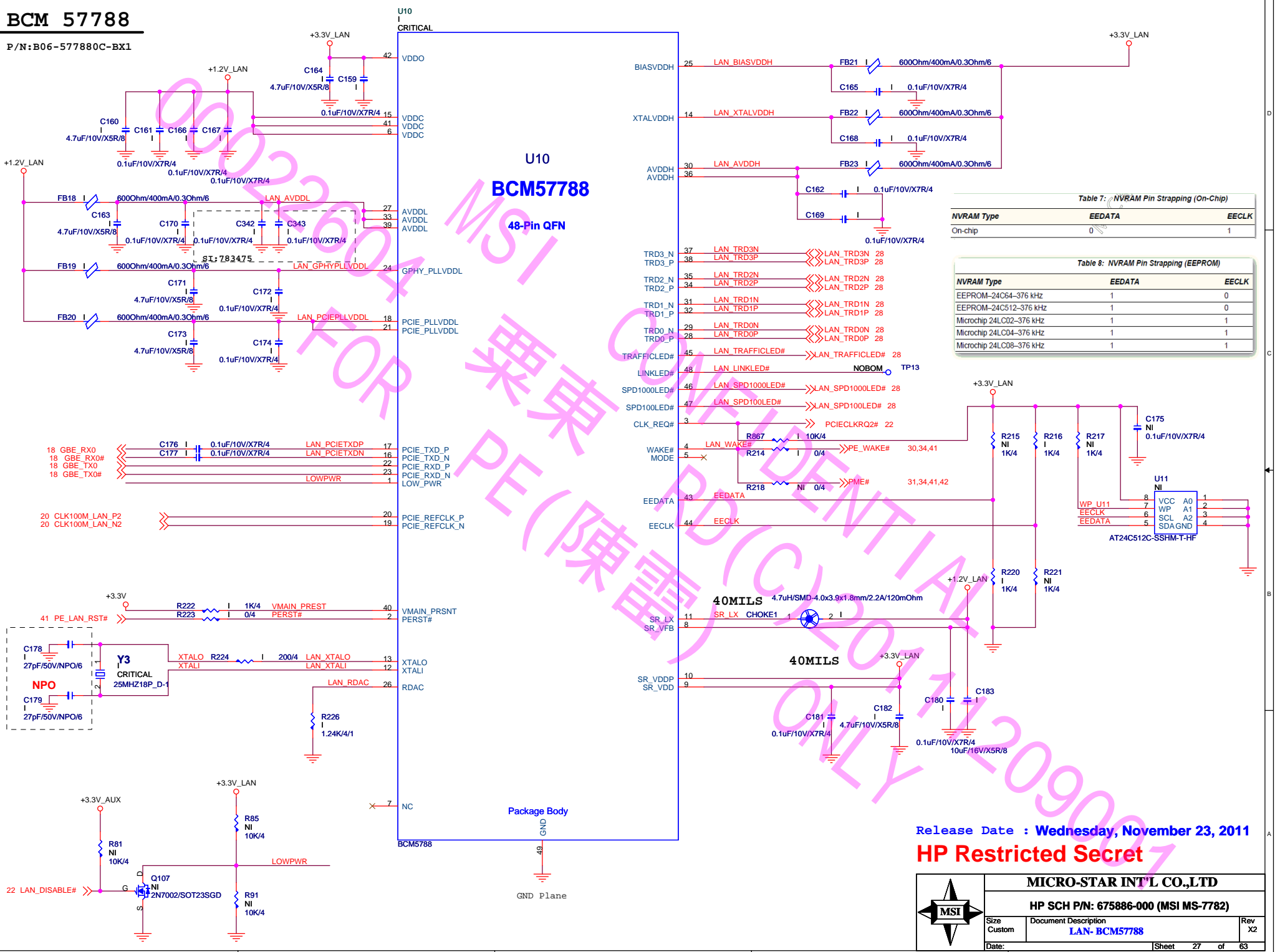
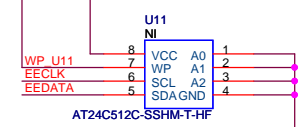


Table 7: NVRAM Pin Strapping (On-Chip)

| NVRAM Type | EEDATA | EECLK |
|------------|--------|-------|
| On-chip | 0 | 1 |

Table 8: NVRAM Pin Strapping (EEPROM)

| NVRAM Type | EEDATA | EECLK |
|--------------------------|--------|-------|
| EEPROM-24C64-376 kHz | 1 | 0 |
| EEPROM-24C512-376 kHz | 1 | 0 |
| Microchip 24LC02-376 kHz | 1 | 1 |
| Microchip 24LC04-376 kHz | 1 | 1 |
| Microchip 24LC08-376 kHz | 1 | 1 |



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HP SCH P/N: 675886-000 (MSI MS-7782)

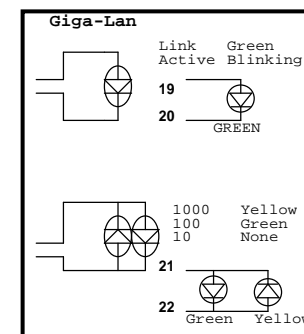
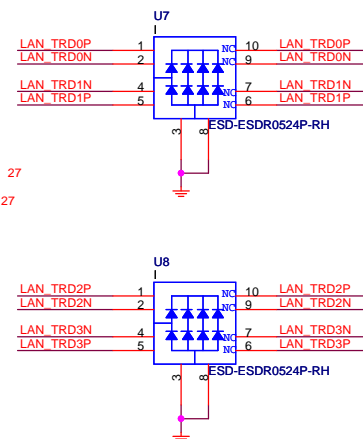
Document Description
LAN- BCM57788

Rev X2

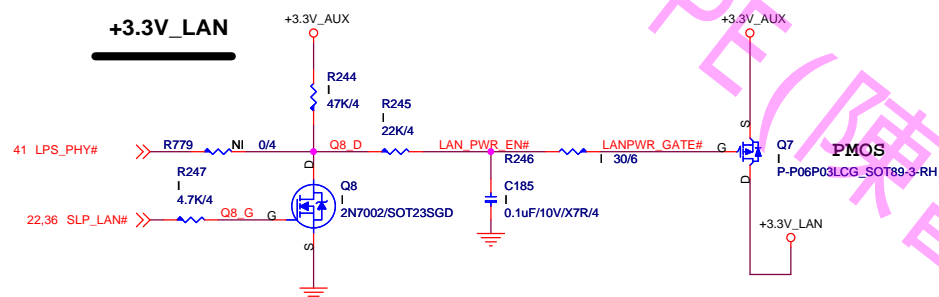
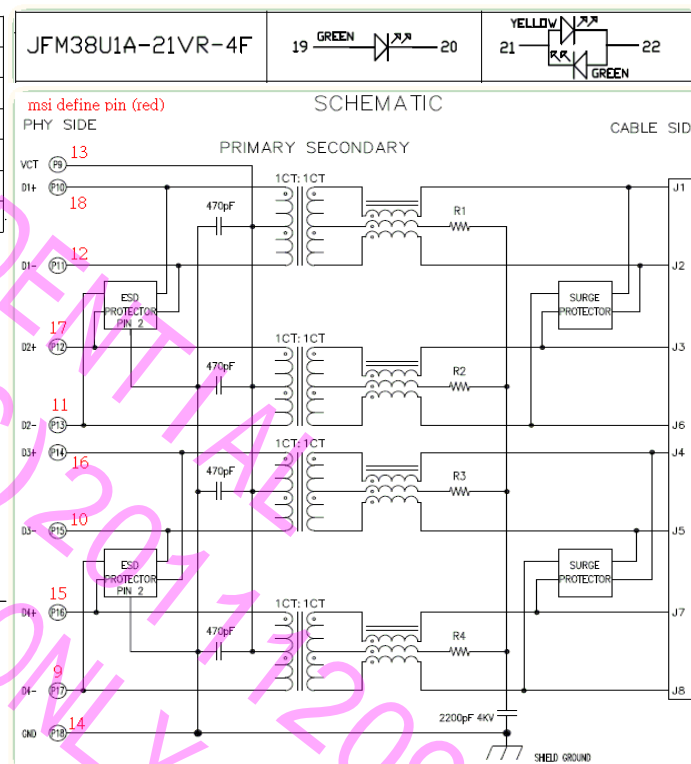
Date:

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P/N:N58-22F1481-U30



| Function | Link LED | Speed LED |
|----------------------|---------------|----------------|
| 10Mb Link | Green (solid) | Off |
| 100Mb Link | Green (solid) | Yellow (solid) |
| 1000Mb Link | Green (solid) | Green (solid) |
| 10Mb Data Transfer | Green (blink) | Off |
| 100Mb Data Transfer | Green (blink) | Yellow (solid) |
| 1000Mb Data Transfer | Green (blink) | Green (solid) |



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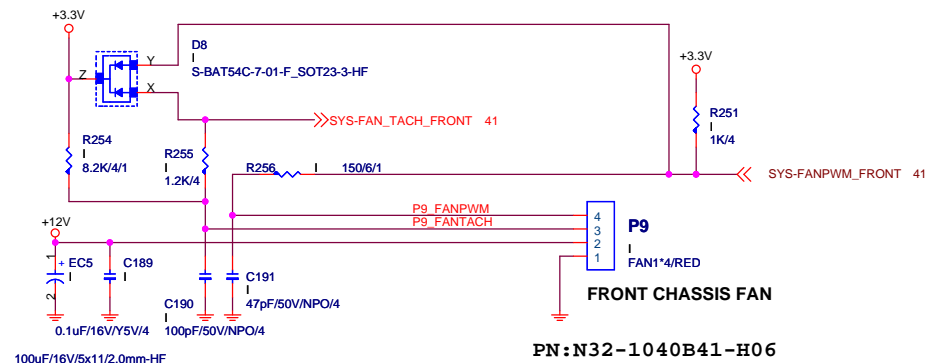
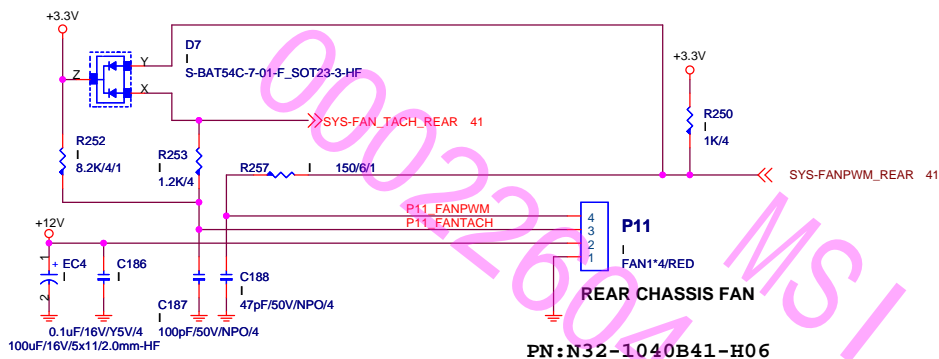
HP SCH P/N: 675886-000 (MSI MS-7782)

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| Size Custom | Document Description LAN POWER/CONN |
|----------------|---|

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| Date: | Sheet 28 of 63 |
|-------|----------------|

FAN BLOCK

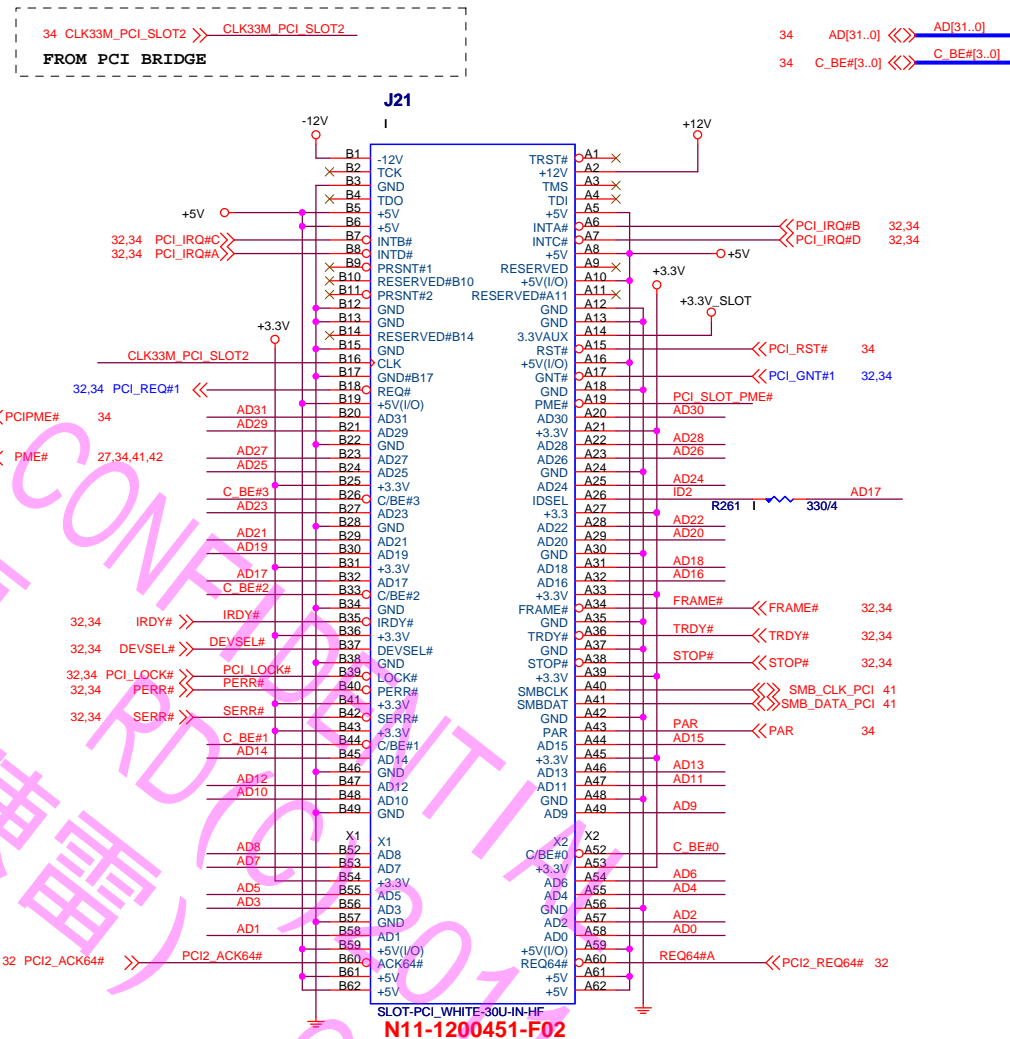


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| MICRO-STAR INT'L CO.,LTD | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | |
| Size Custom | Document Description |
| | FAN |
| Date: | Rev X2 |



PCI SLOT 1 (PCI VER: 2.3 COMPLY)

PCI_SLOT2
IDSEL = AD17
PCI_REQ#1
PCI_GNT#1
PCI_INTB#

HP Restricted Secret

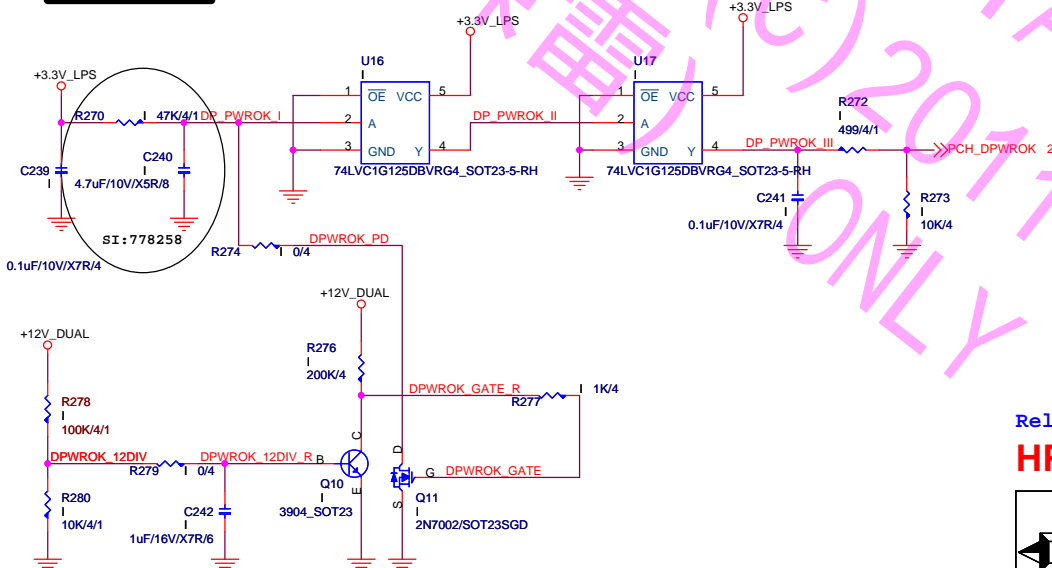
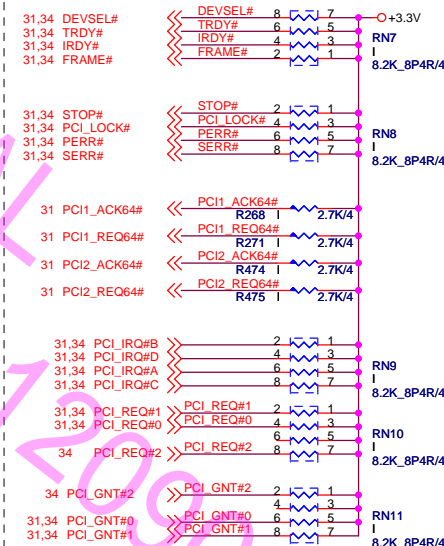
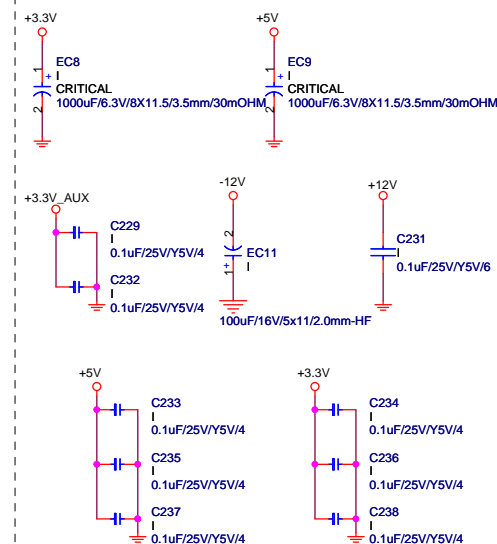
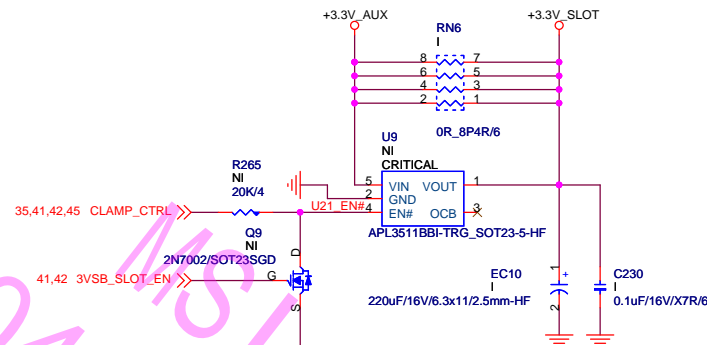
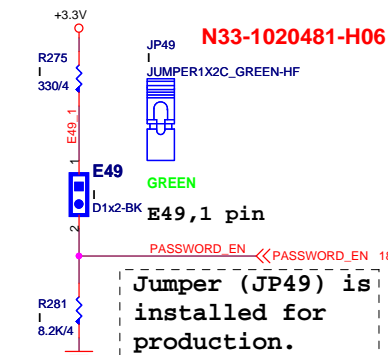
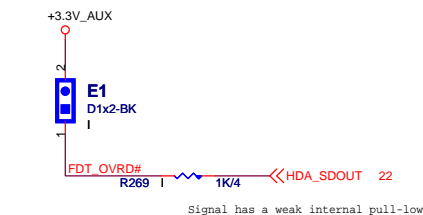
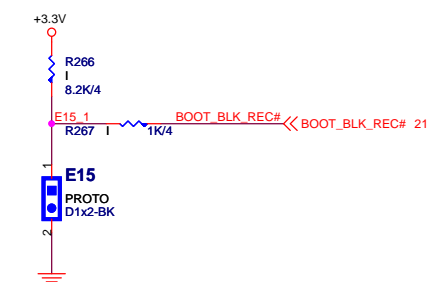
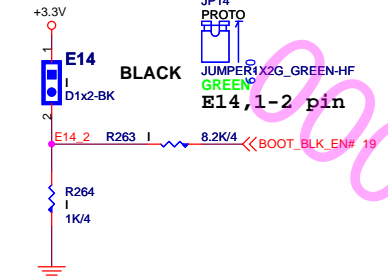


HP SCH P/N: 675886-000 (MSI MS-7782)

| Size | Document Description |
|--------|----------------------|
| Custom | PCI SLOT |

| | |
|--|-----------|
| | Rev X2 |
|--|-----------|

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| Date: | Sheet 31 of 63 |
|-------|----------------|

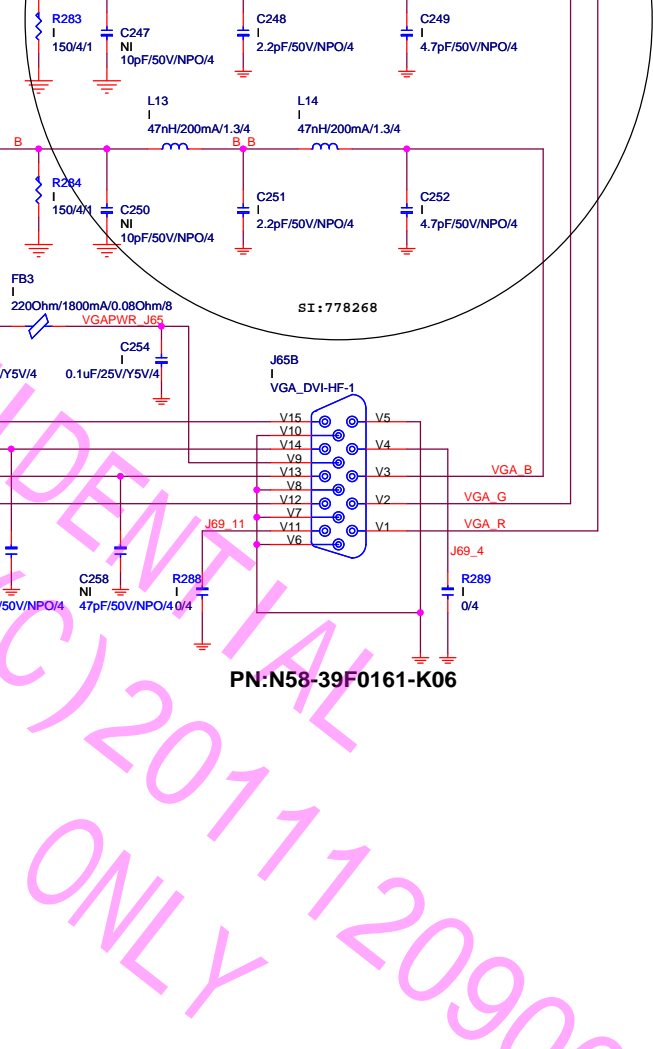
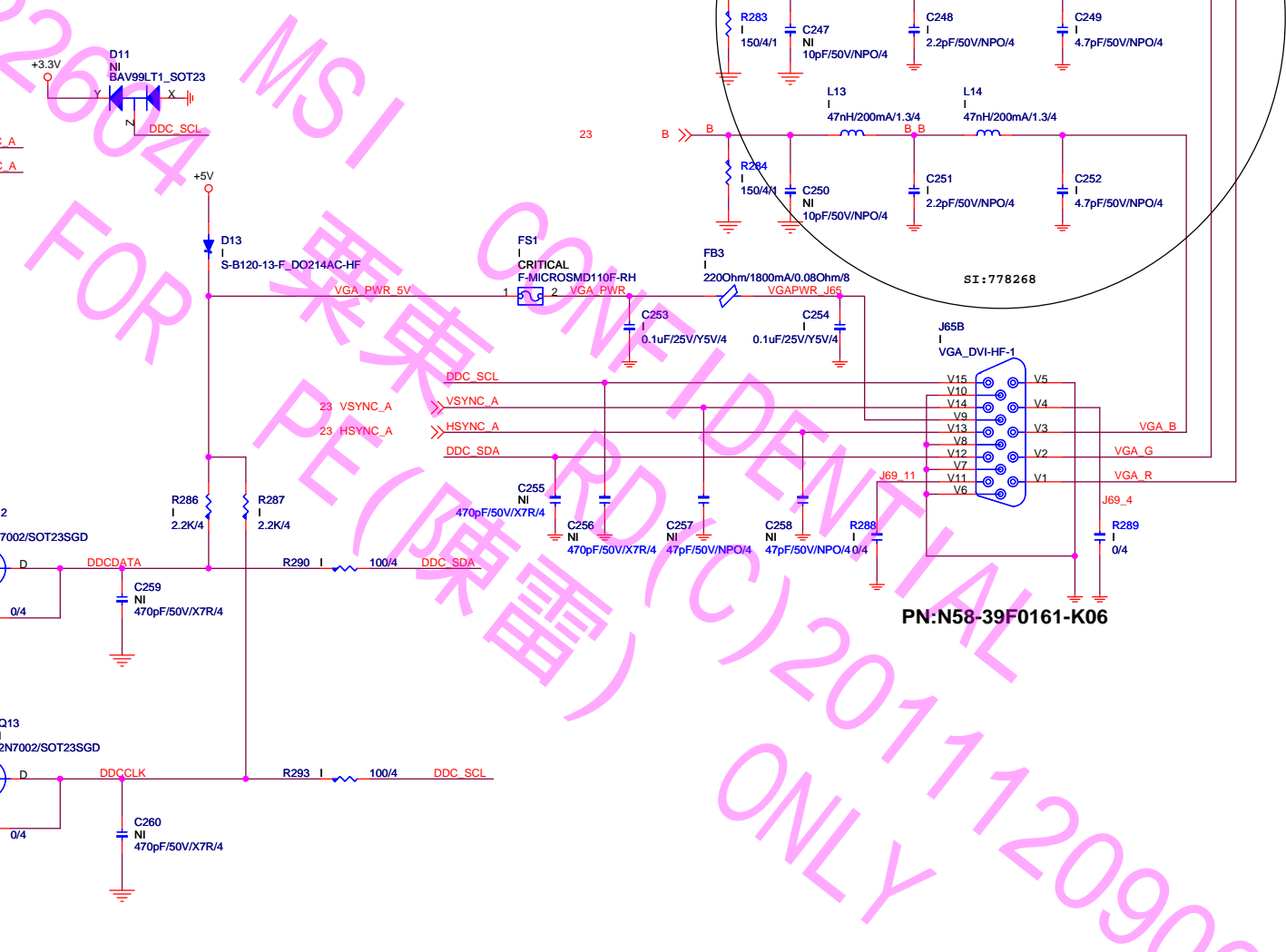


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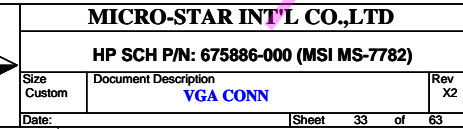


| | | |
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| Size Custom | Document Description PCI pull U D/+3V_SLOT/DPWROK | Rev X2 |
| Date: | Sheet 32 of 63 | |

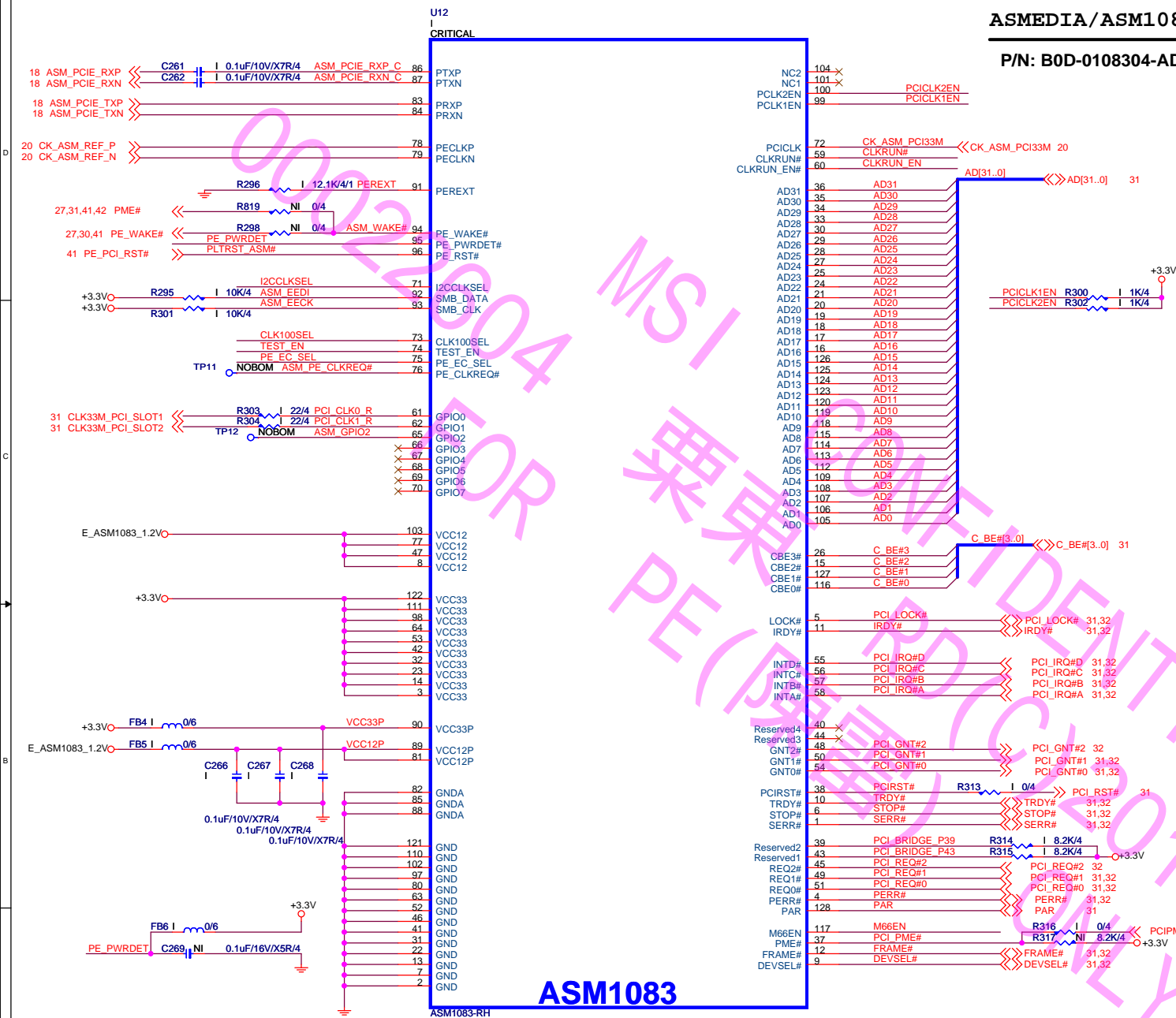
MS/



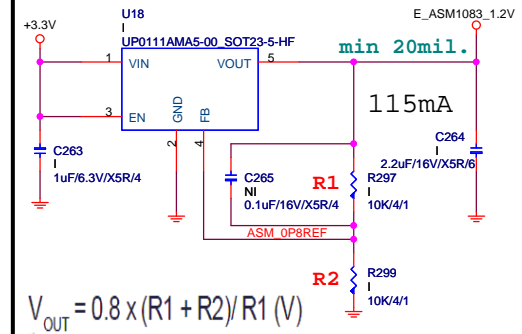
Release Date : Wednesday, November 23, 2011
HP Restricted Secret



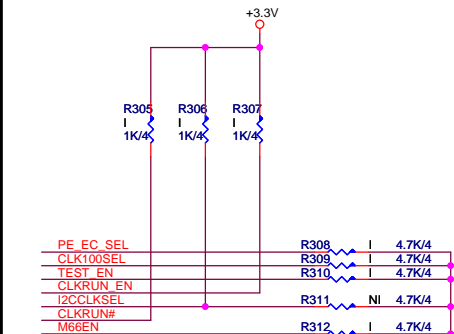
P/N: B0D-0108304-AD0



E_ASM1083_1.2V



H/W Strapping



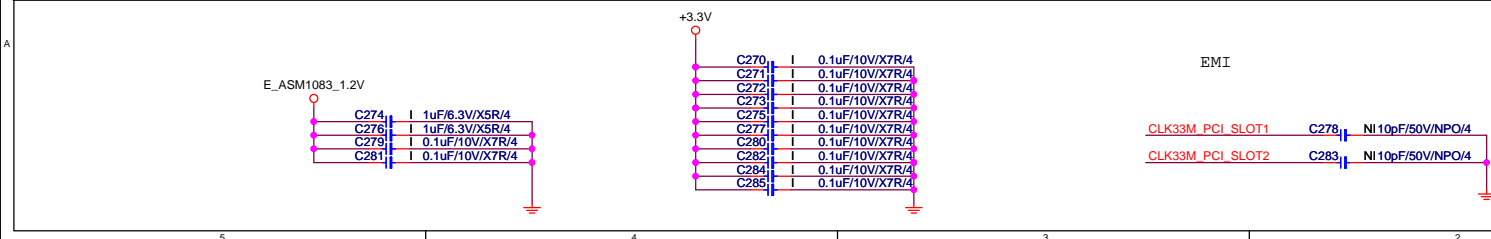
```
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
```

CLK100SEL-
 "H" for PECLK input only
 "L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
 "H" is 135KHz I2CCLK
 "L" is 67.5KHz I2CCLK



Release Date : **Wednesday, November 23, 2011**

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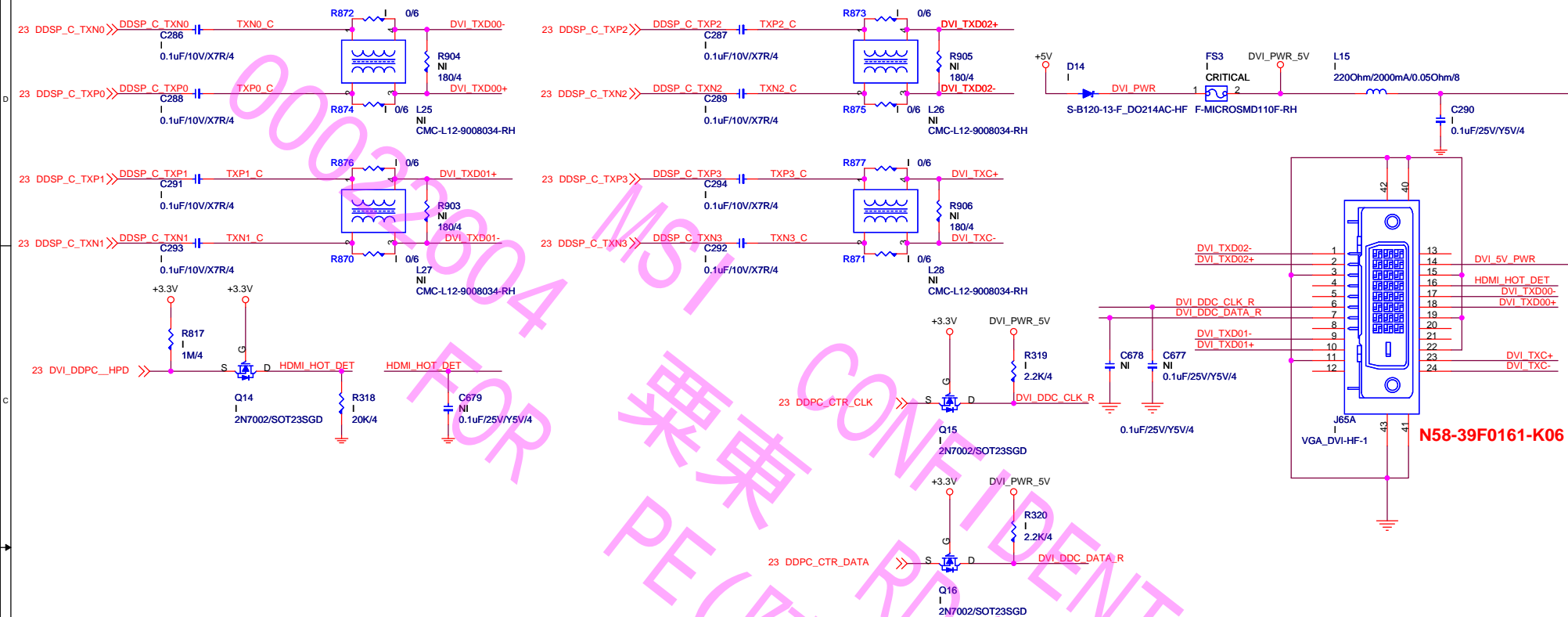


MICRO-STAR INT'L CO.,LTD

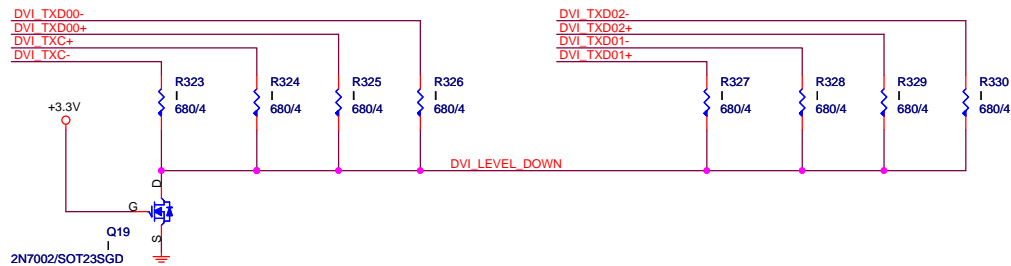
HP SCH P/N: 675886-000 (MSI MS-7782)

| | | |
|----------------|---|-----------|
| Size Custom | Document Description PCIe to PCI Bridge | Rev X2 |
| Date: | Sheet 34 of 63 | |

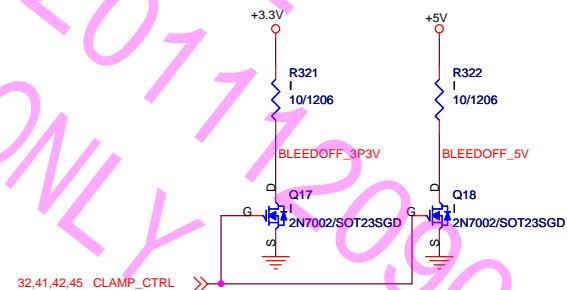
DVI Connector



DVI Level Shift



BLEED-OFF CIRCUIT

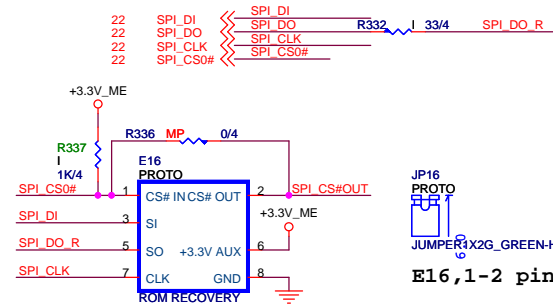


Release Date : Wednesday, November 23, 2011

HP Restricted Secret

| | | | |
|--------------------------------------|---|--|-----------|
| MICRO-STAR INT'L CO.,LTD | | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | | |
| Size Custom | Document Description DVI / BLEED OFF | | Rev X2 |
| Date: | Sheet 35 of 63 | | |

PN:M31-25L6442-M24

TABLE 22
ROM RECOVERY HEADER DEFINITION

| PIN # | SIGNAL NAME | SIGNAL NAME | PIN # |
|-------|-------------|-----------------|-------|
| 1 | CS# IN | CS# OUT | 2 |
| 3 | SI | KEY (no pin) | 4 |
| 5 | SO | VCC (+3.3V AUX) | 6 |
| 7 | CLK | GND | 8 |

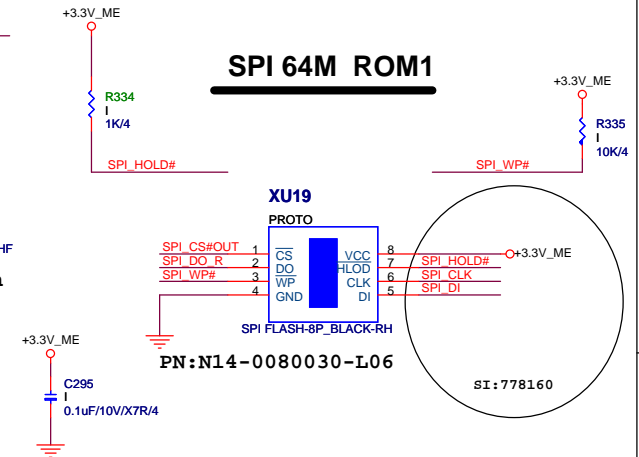
XU19

PROTO

| Pin | Signal |
|-----|------------|
| 1 | SPI_CS#OUT |
| 2 | SPI_DO R |
| 3 | SPI_WP# |
| 4 | GND |
| 5 | DI |
| 6 | CLK |
| 7 | HLOD |
| 8 | VCC |

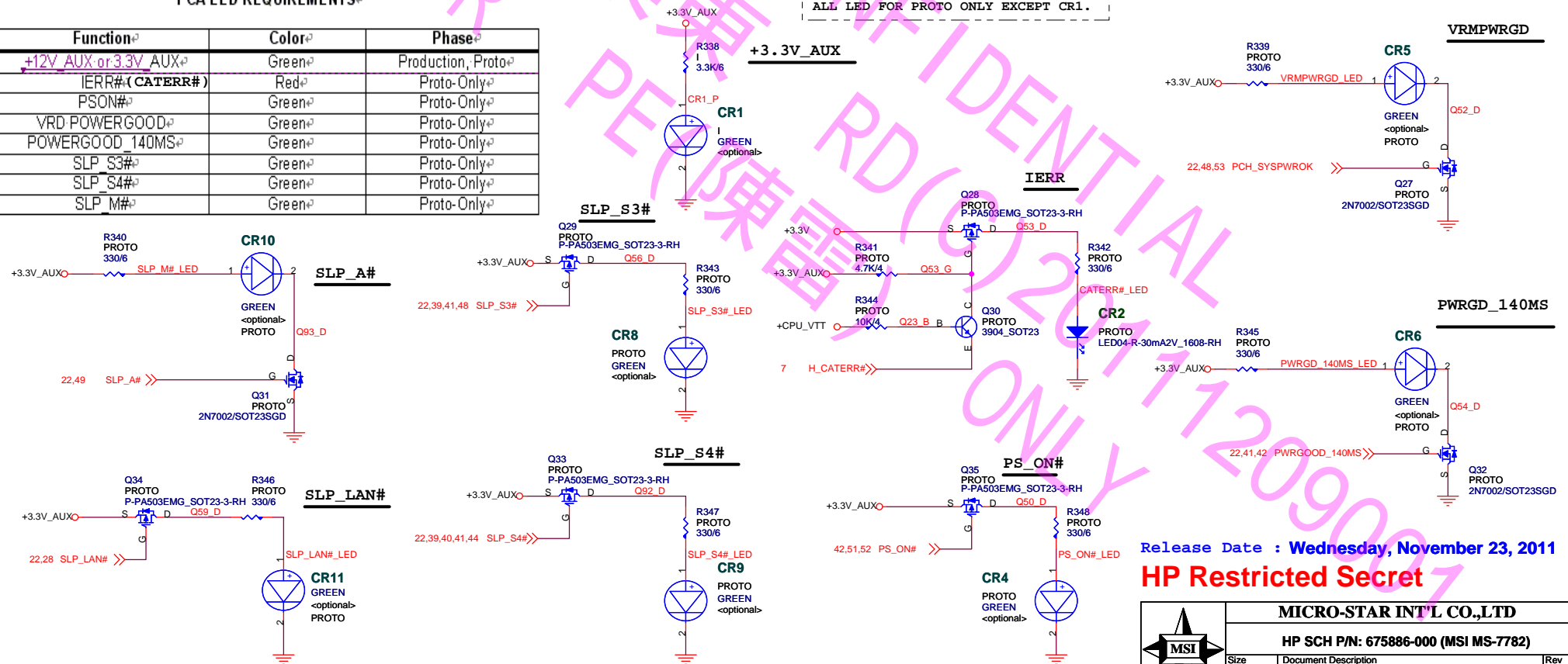
SPI FLASH-8P_BLACK-RH

PN:N14-0080030-L06



ALL LED FOR PROTO ONLY EXCEPT CR1.

| Function | Color | Phase |
|----------------------|-------|-------------------|
| +12V_AUX or 3.3V_AUX | Green | Production, Proto |
| IERR# (CATERR#) | Red | Proto-Only |
| PSON# | Green | Proto-Only |
| VRD_POWERGOOD | Green | Proto-Only |
| POWERGOOD_140MS | Green | Proto-Only |
| SLP_S3# | Green | Proto-Only |
| SLP_S4# | Green | Proto-Only |
| SLP_M# | Green | Proto-Only |



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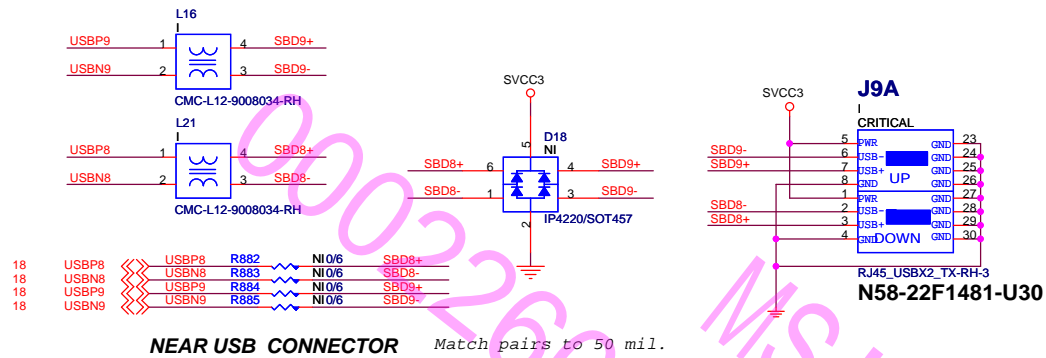
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

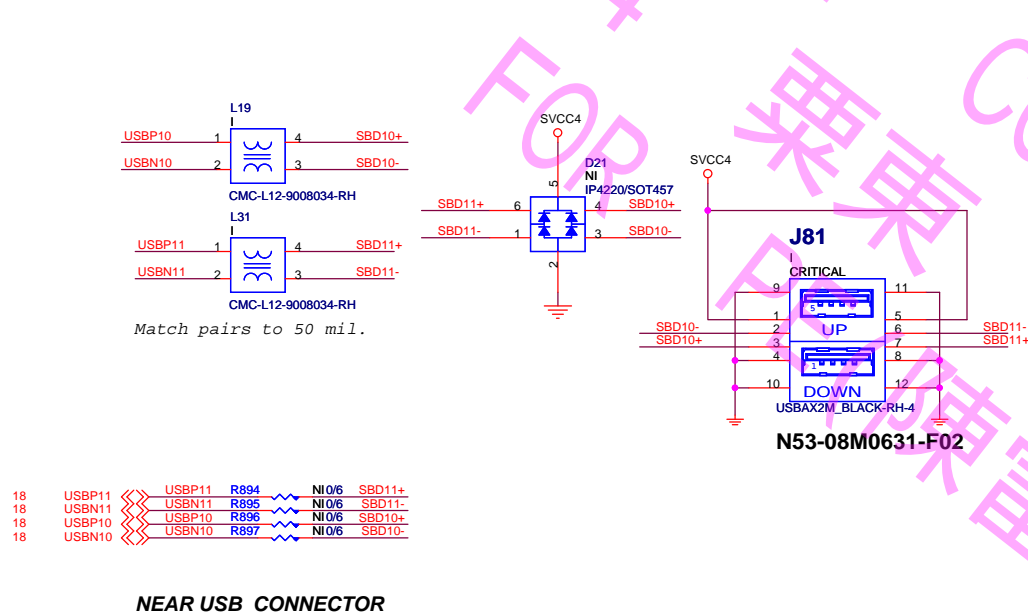
| | |
|--------|----------------------|
| Size | Document Description |
| Custom | SPI ROM / LED |

| | |
|-------|----------------|
| Date: | Sheet 36 of 63 |
|-------|----------------|

REAL USB CONNECTOR WITH RJ45 FOR USB PORT 8,9



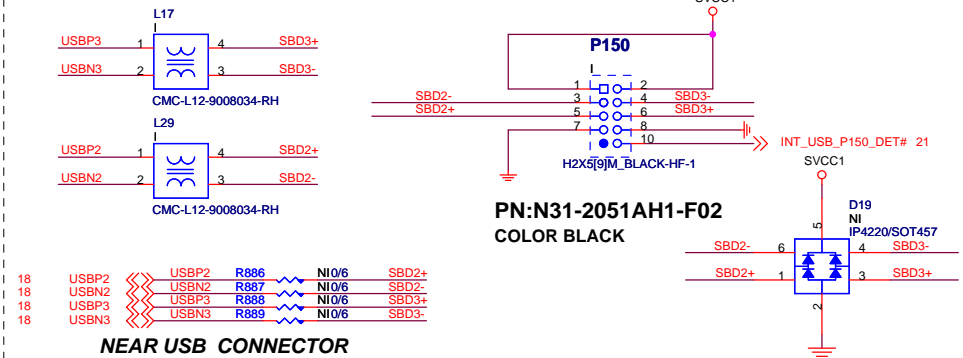
REAR PANEL USB CONNECTOR FOR USB PORT 10,11



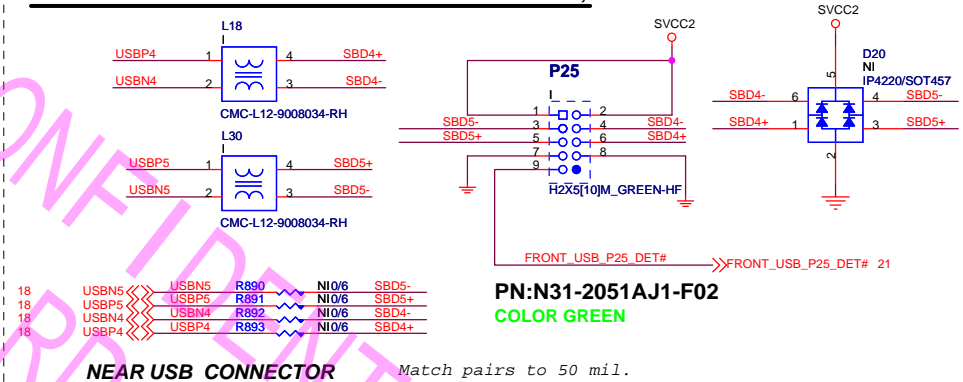
USBP11 USBN11 USBP10 USBN10 R894 R895 R896 R897 NI/O/6 SBD11+ SBD11- SBD10+ SBD10-

FRONT_USB_P24_DET# R349 10K/4
INT_USB_P150_DET# R350 10K/4
FRONT_USB_P25_DET# R351 10K/4

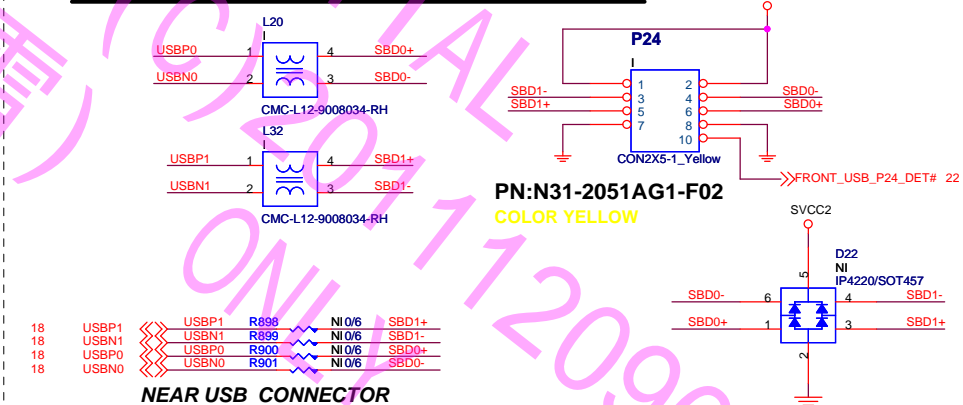
INTERNAL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

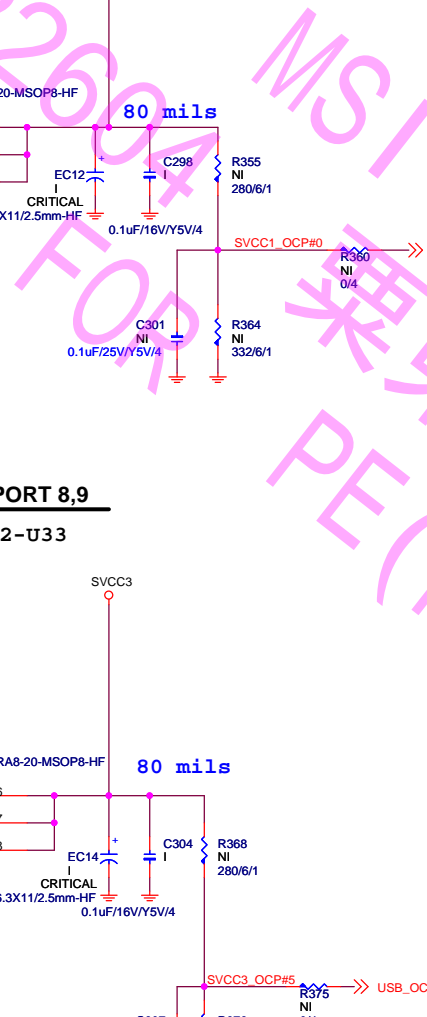


Release Date : Wednesday, November 23, 2011

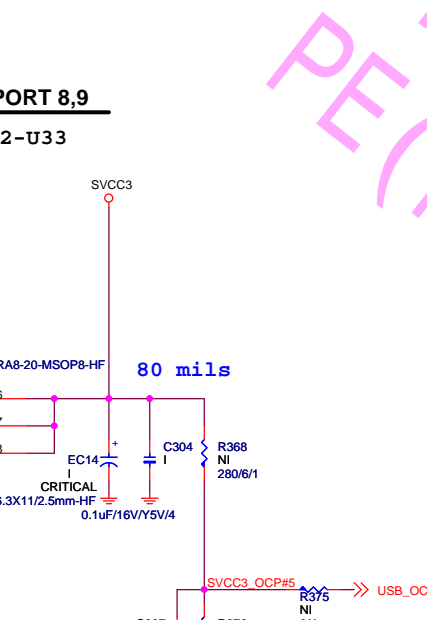
HP Restricted Secret

| | | |
|--------------------------------------|--------------------------------|--------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description USB Conn. | Rev X2 |
| Date: | Sheet 37 of 63 | |

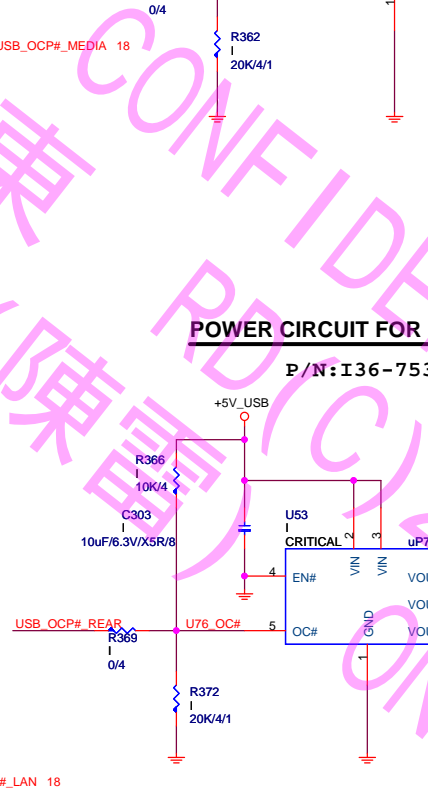
P/N: I36-7534B02-U33



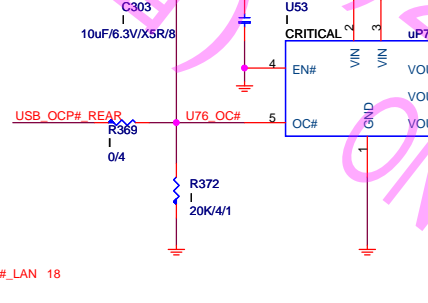
P/N: I36-7534B02-U33



P/N:I36-7534B02-U33



P/N: I36-7534B02-U33



HP Restricted Secret



HP SCH P/N: 675886-000 (MSI MS-7782)

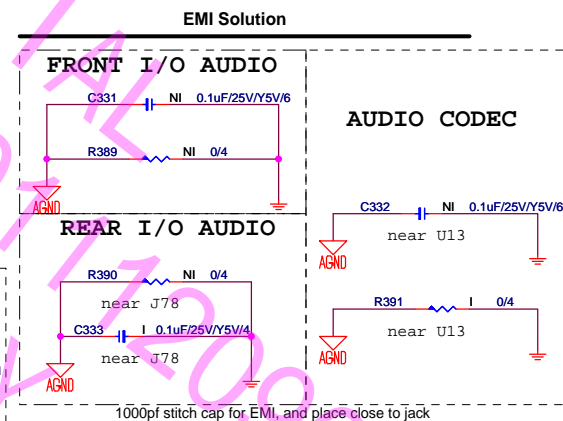
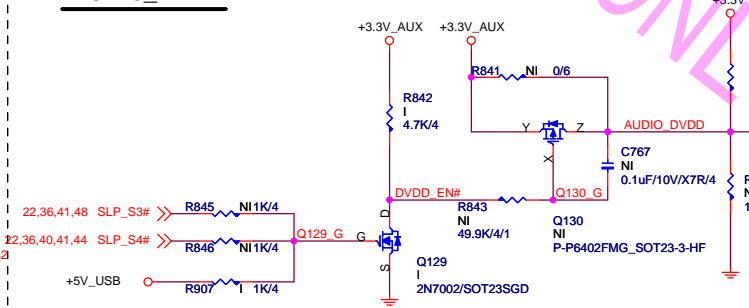
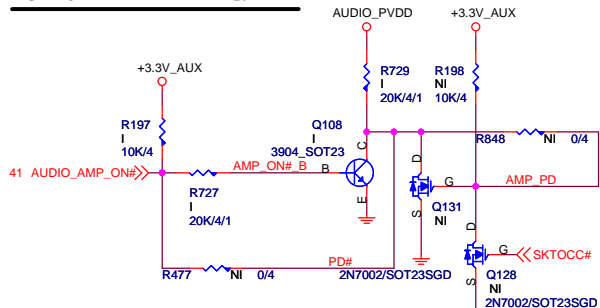
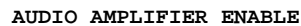
| | |
|--|----|
| | Re |
|--|----|

| | |
|-------|----------------|
| Date: | Sheet 38 of 63 |
|-------|----------------|

PN:B05-LC2210C-R09



All of JD resistors should be placed as close as possible to the sense pin of codec.



Release Date : Wednesday, November 23, 2011

HP Restricted Secret



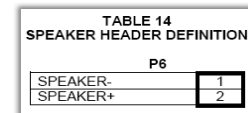
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

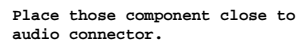
| | | |
|----------------|--|----|
| Size Custom | Document Description ALC 221 CODEC | Re |
| Date: | Sheet 39 of 63 | |

SPEAKER HEADER

P/N:N32-10200D1-F02



```
SPK+- TRACE WIDTH
Speaker 4 ohm ==> 40mils
Speaker 8 ohm ==> 20mils
```



HP Restricted Secret



MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

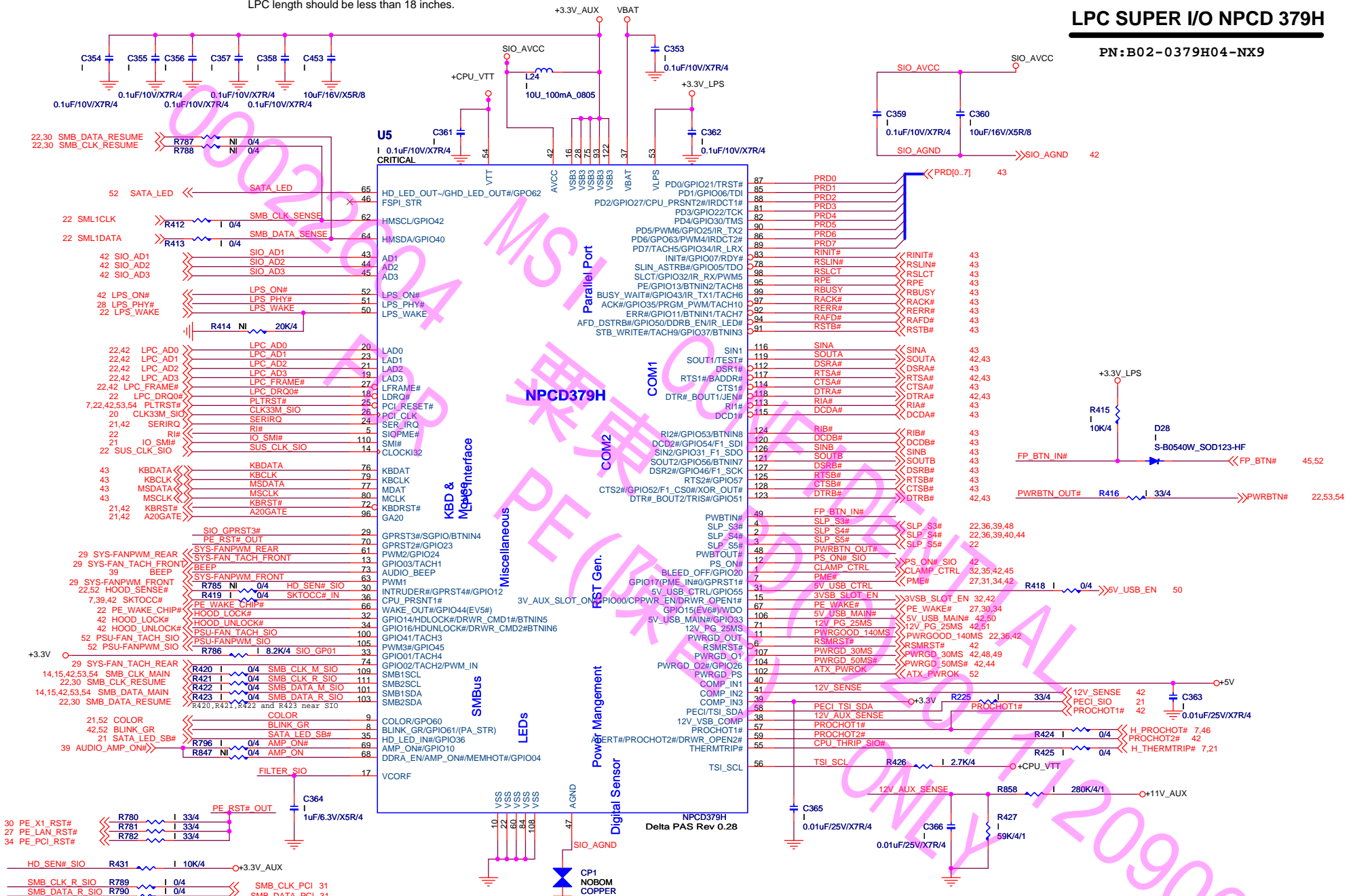
| | |
|--------|------------------------|
| Size | Document Description |
| Custom | Audio Connector |

| | |
|----|--|
| Re | |
|----|--|

LPC length should be less than 18 inches.

LPC SUPER I/O NPCD 379H

PN:B02-0379H04-NX9



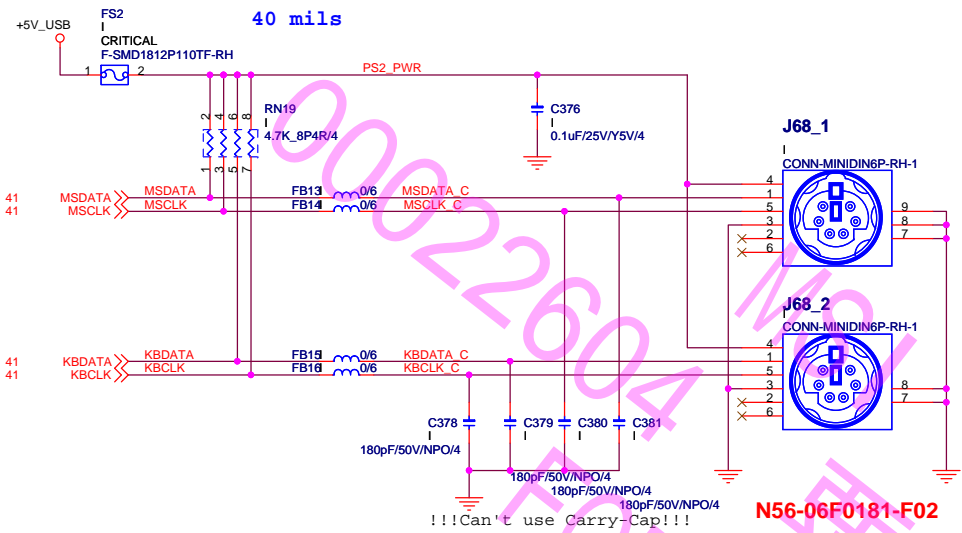
Release Date : Wednesday, November 23, 2011

HP Restricted Secret

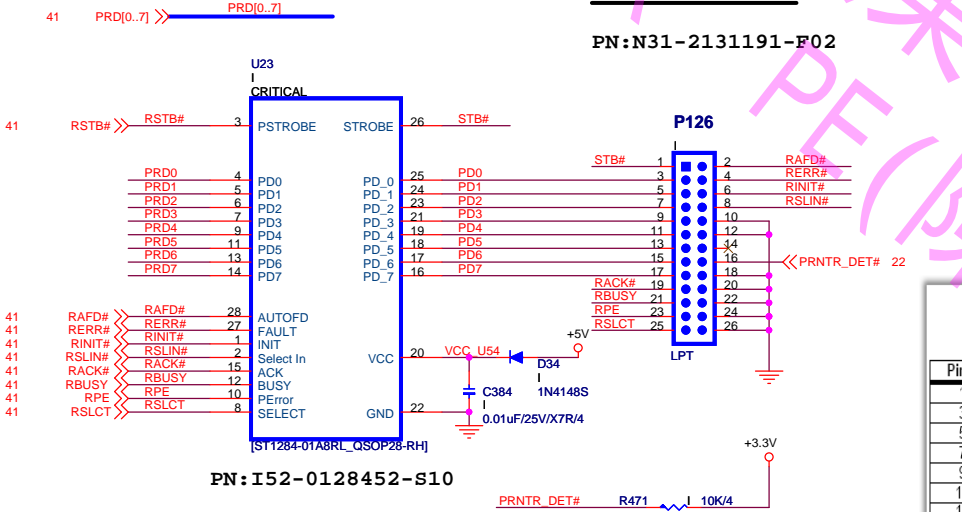
| | | |
|--------------------------------------|----------------------|--------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| LPC SUPER I/O NPCD379H | | |
| Size Custom | Document Description | Rev X2 |
| Date: | Sheet 41 of 63 | |



PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT

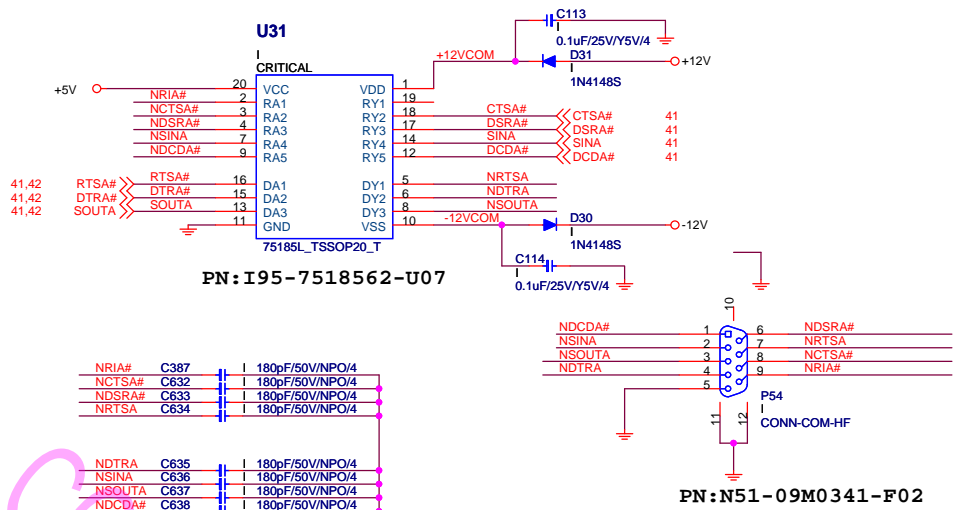


Parallel Port 2 x13 header

| PIN # | SIGNAL NAME | SIGNAL NAME | PIN # |
|-------|-------------|-------------|-------|
| 1 | LPT_STB# | XAFD# | 2 |
| 3 | LPT_SPD0 | ERROR# | 4 |
| 5 | LPT_SPD1 | XINIT# | 6 |
| 7 | LPT_SPD2 | XSLIN# | 8 |
| 9 | LPT_SPD3 | GND | 10 |
| 11 | LPT_SPD4 | GND | 12 |
| 13 | LPT_SPD5 | GND | 14 |
| 15 | LPT_SPD6 | PRT_DET# | 16 |
| 17 | LPT_SPD7 | GND | 18 |
| 19 | ACK# | GND | 20 |
| 21 | BUSY | GND | 22 |
| 23 | PE | LDT_RST# | 24 |
| | SLCT | GND | 26 |

| | | |
|--------|------|--------------------|
| PD0 | C668 | NI 180pF/50V/NPO/4 |
| PD1 | C662 | NI 180pF/50V/NPO/4 |
| PD2 | C664 | NI 180pF/50V/NPO/4 |
| PD3 | C665 | NI 180pF/50V/NPO/4 |
| PD4 | C666 | NI 180pF/50V/NPO/4 |
| PD5 | C667 | NI 180pF/50V/NPO/4 |
| PD6 | C661 | NI 180pF/50V/NPO/4 |
| PD7 | C663 | NI 180pF/50V/NPO/4 |
| STB# | C676 | NI 180pF/50V/NPO/4 |
| RACK# | C670 | NI 180pF/50V/NPO/4 |
| RBUSY | C672 | NI 180pF/50V/NPO/4 |
| RPE | C673 | NI 180pF/50V/NPO/4 |
| RSLCT | C674 | NI 180pF/50V/NPO/4 |
| RAFD# | C675 | NI 180pF/50V/NPO/4 |
| RERR# | C669 | NI 180pF/50V/NPO/4 |
| RSLIN# | C671 | NI 180pF/50V/NPO/4 |

SERIAL PORT 1



SERIAL PORT 2

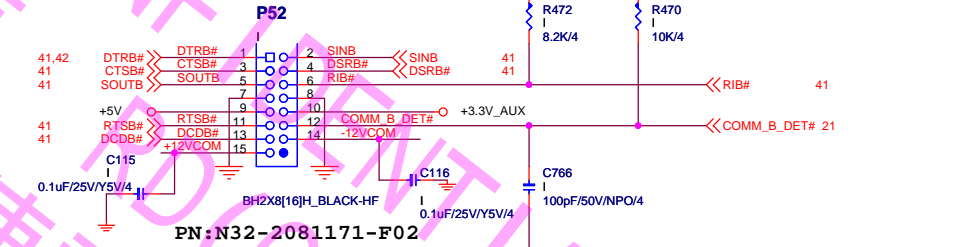
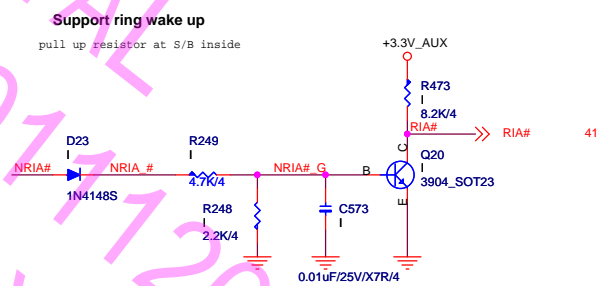


TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

| Pin # | Signal Name | Signal Name | Pin # |
|-------|--------------------|--------------------|-------|
| 1 | DTR# | RXD | 2 |
| 3 | CTS# | DSR# | 4 |
| 5 | TXD | R# | 6 |
| 7 | GND | GND | 8 |
| 9 | +5 V | +3.3 VAUX | 10 |
| 11 | RTS# | COMM B DETECT# | 12 |
| 13 | DCD# | -12 V (THRU DIODE) | 14 |
| 15 | +12 V (THRU DIODE) | KEY | 16 |



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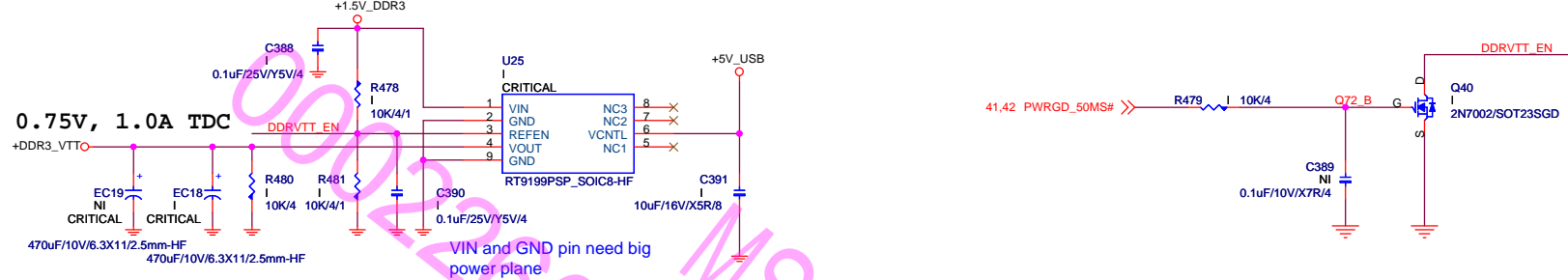
HP SCH P/N: 675886-000 (MSI MS-7782)

Size Custom Document Description
KB / MS / COM / LPT

Date: Sheet 43 of 63

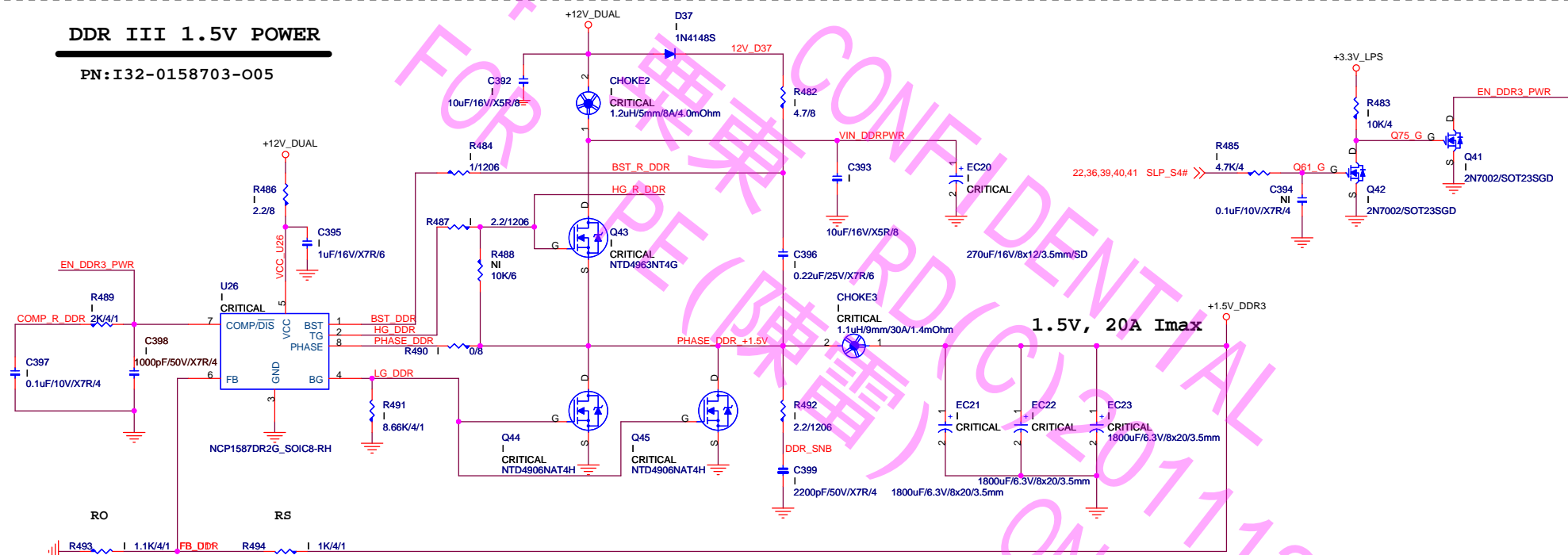
DDR VTT Power

PN: I31-0919902-R11

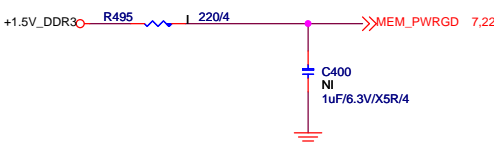


DDR III 1.5V POWER

PN: I32-0158703-O05




MEM_PWRGD

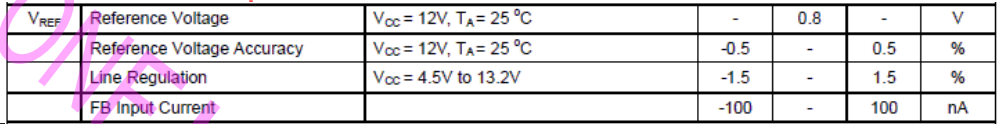


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| | | | |
|---|---|----------------------|--------|
|  | MICRO-STAR INT'L CO.,LTD | | |
| | HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| | Size Custom | Document Description | Rev X2 |
| | +1.5V_DDR3 / DDRVTT | | 63 |
| | Date: | Sheet 44 of | |

P/N: I31-5611C09-A30



+5V_USB_SUS_ACK

22 SUS_PWR_ACK# << R509 I 0/4 SUS_PWRACK#

+3.3V_AUX +3.3V_LPS

R512 NI 100K/4 R513 I 10K/4

SUS_ACK#_GATE Q50 2N7002/SOT23SGD

SUS_5V_ACK# SUS_5V_ON# SUS_5V_ON#_GATE Q51 2N7002/SOT23SGD

R514 I 0/4 R517 NI 10K/4

R518 I 2.2K/4

+5V_USB R519 10K/4

Q52 3904_SOT23

R520 I 10K/4

C409 NI 0.1uF/10V/X7R/4

R521 I 2.67K/4/1

C410 0.1uF/10V/X7R/4

32,35,41,42 CLAMP_CTRL >> Q53 2N7002/SOT23SGD

SUS_WARN#_ACK# SUS_WARN#_R R522 I 0/4

41,52 FP_BTN# >> Q54 2N7002/SOT23SGD

22 SUS_WARN# >>

+3.3V_ME

+3.3V_LAN +3.3V_ME

R508 NI 0/8

22,49 SLP_A >> R515 I 10K/4

3VME_GATE Q49 PMOS P-P06P03LCG_SOT89-3-RH

C407 1uF/6.3V/X5R/4

+3.3V_AUX +3.3V_ME

For board bring up, and to insure that the handshake circuit does not prevent the circuit from going into DeepSleep, do the following:

R667 Installed

R509 Non-installed

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| | | |
|--|--------------------------------------|---|
| | MICRO-STAR INT'L CO.,LTD | |
| | HP SCH P/N: 675886-000 (MSI MS-7782) | |
| | Size Custom | Document Description CPU SA POWER/+3.3V_ME |
| | | Rev X2 |

HP Restricted Secret

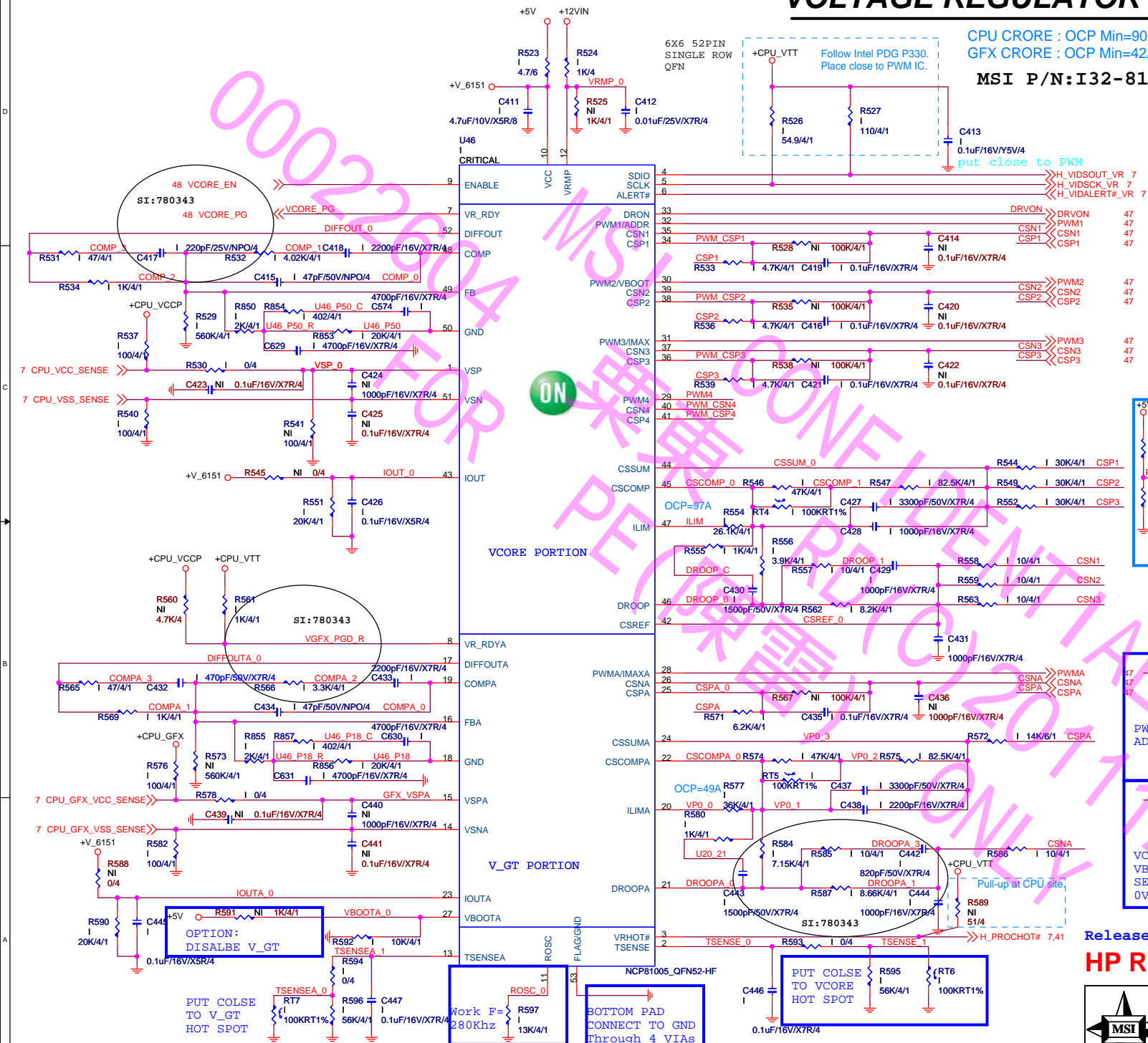


| | | |
|----------------|--|-----------|
| Size Custom | Document Description CPU SA POWER/+3.3V_ME | Rev X2 |
| Date: | Sheet 45 of 63 | |

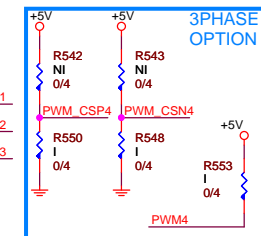
VOLTAGE REGULATOR MODULE (VRD12)

CPU CRORE : OCP Min=90A , OCP Max=108A , OVP=DAC+175mV
GFX CRORE : OCP Min=42A , OCP Max=52.5A , OVP=DAC+175mV

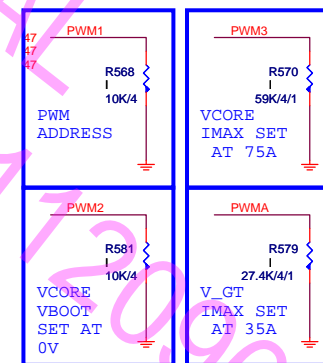
MSI P/N:I32-810050C-005



| PWM ADDRESS | | |
|-------------------|-----------------------------------|----------------------------------|
| RESISTOR VALUE | SVID ADDRESS FOR VCORE RAIL | SVID ADDRESS FOR V_GT RAIL |
| 10K | 0000 | 0001 |
| 25K | 0010 | 0011 |
| 45K | 0100 | 0101 |
| 70K | 0110 | 0111 |
| 95K | 1000 | 1001 |
| 125K | 1010 | 1011 |
| 165K | 1100 | 1101 |



| BOOT VOLTAGE | |
|-------------------|-----------------|
| RESISTOR VALUE | BOOT VOLTAGE |
| 10K | 0V |
| 25K | 0.9V |
| 45K | 1V |
| 70K | 1.1V |
| 95K | 1.2V |
| 125K | 1.35V |
| 165K | 1.5V |



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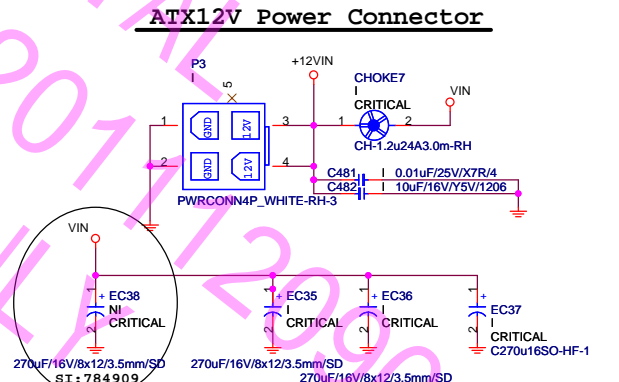
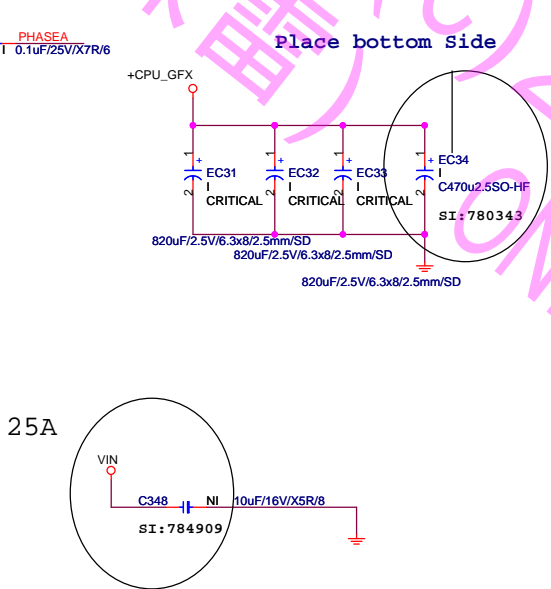
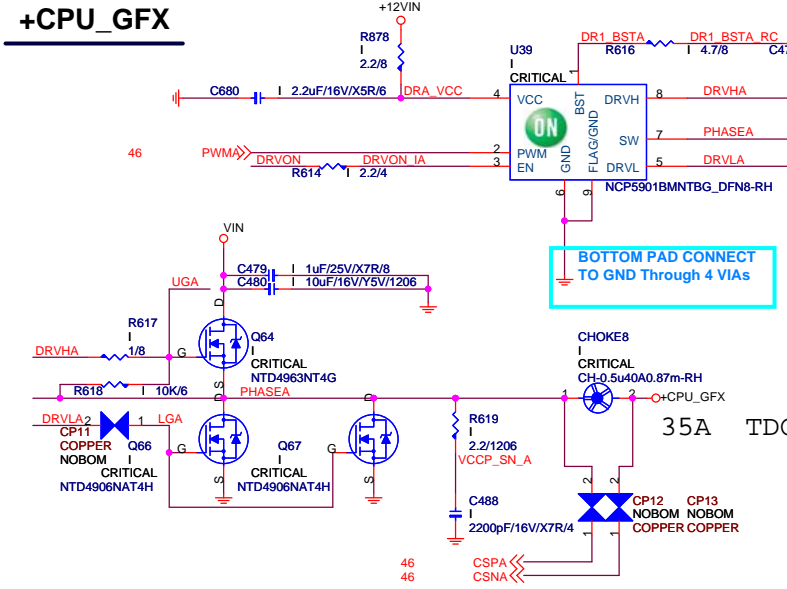
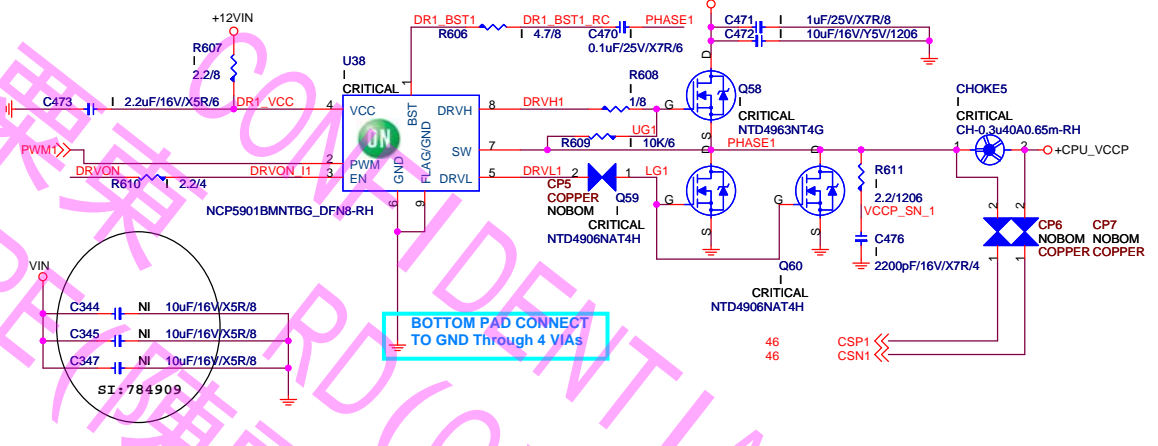
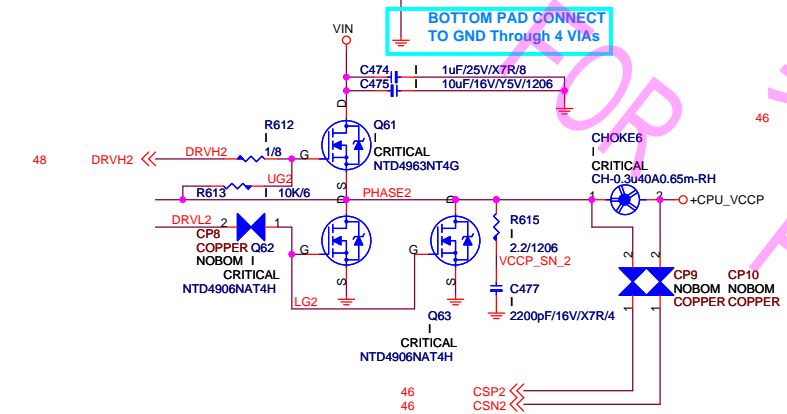
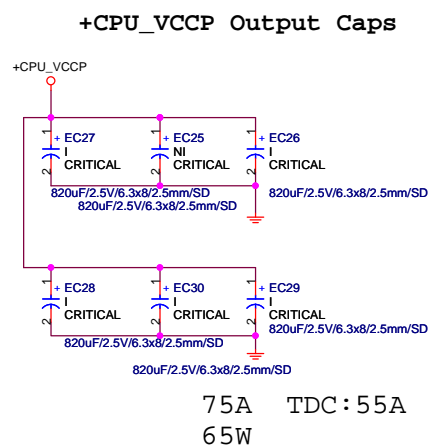
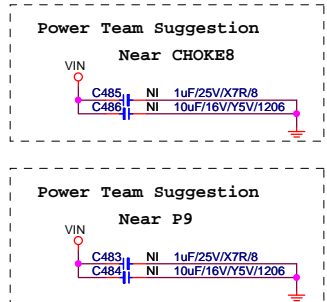
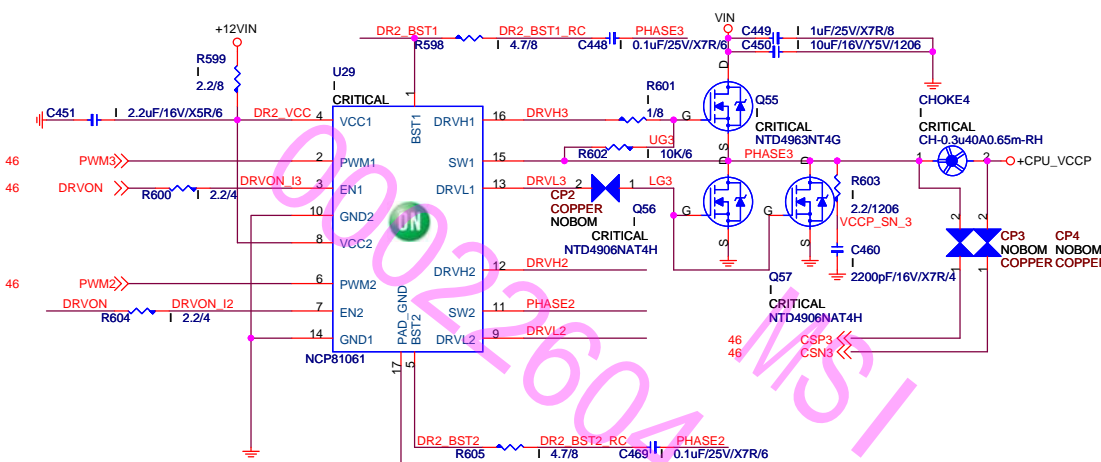
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

| | |
|--------|----------------------|
| Size | Document Description |
| Custom | VRM-NCP81005 |

Rev

| | |
|-------|----------------|
| Date: | Sheet 46 of 63 |
|-------|----------------|



Release Date : Wednesday, November 23, 2011

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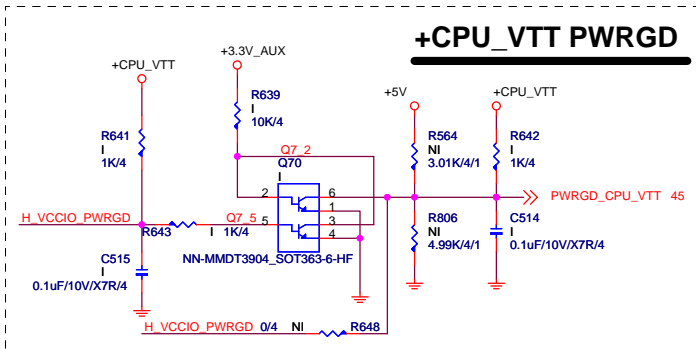
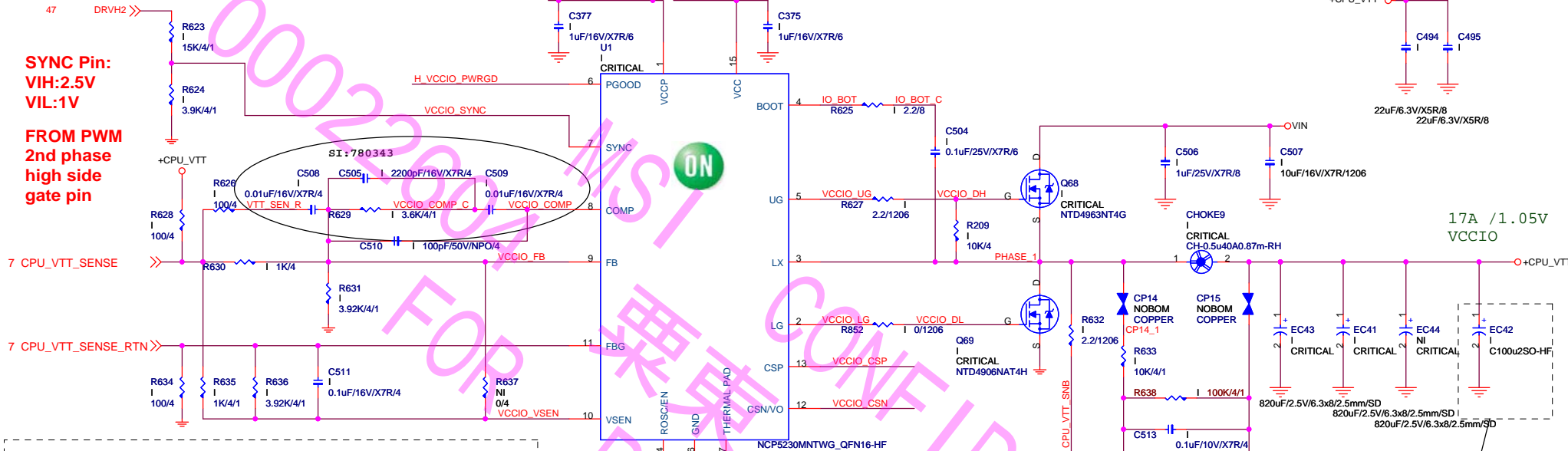
| | | |
|--------------------------------------|----------------------|--------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description | Rev X2 |
| VRM DRIVER-NCP81061 | | |
| Date: | Sheet 47 | of 63 |

CPU VTT Power

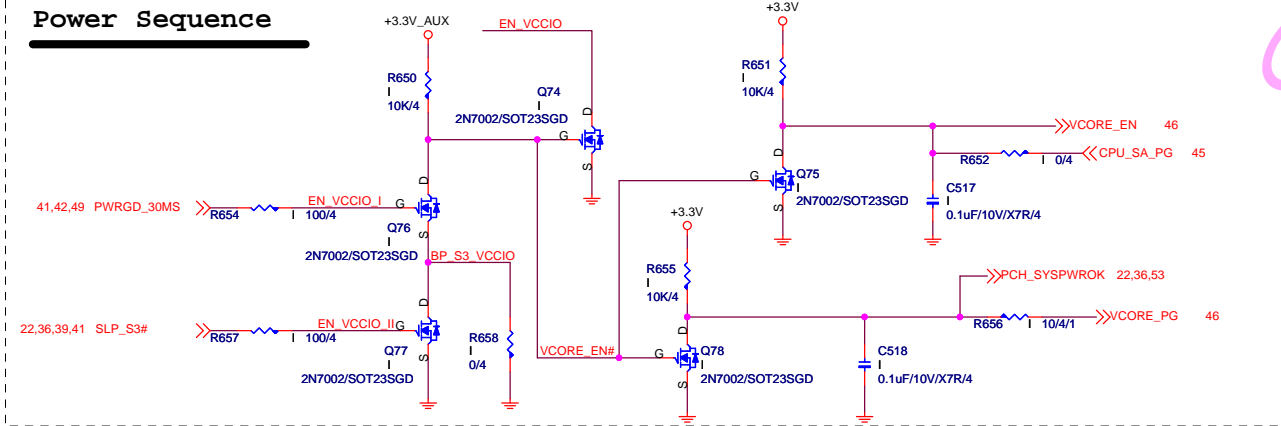
P/N: I32-5230M0C-O05

SYNC Pin:
VIH:2.5V
VIL:1V

FROM PWM
2nd phase
high side
gate pin



Power Sequence

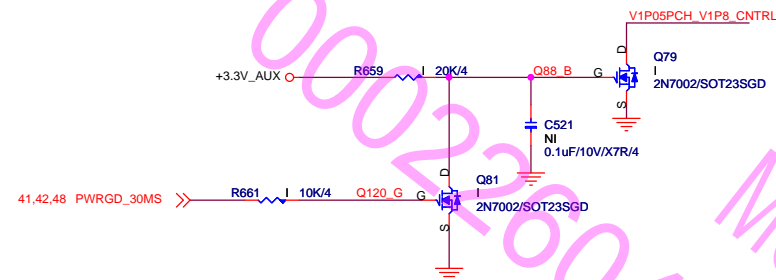


Release Date : Wednesday, November 23, 2011

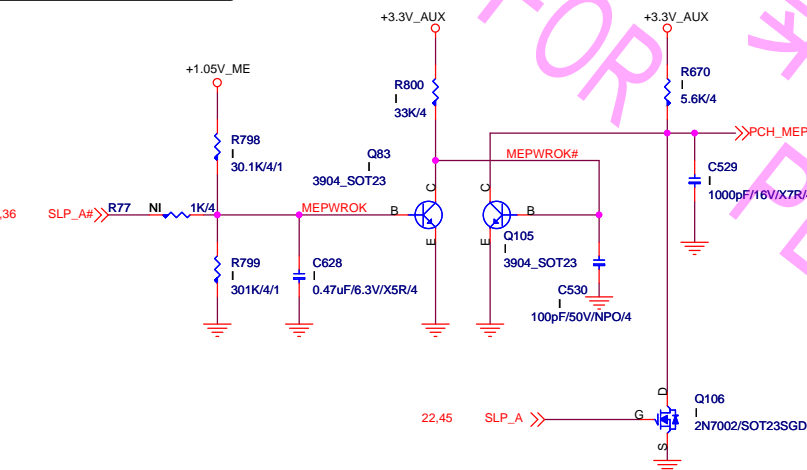
HP Restricted Secret

| | | | |
|--------------------------------------|----------------------|--|--------|
| MICRO-STAR INT'L CO.,LTD | | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | | |
| Size Custom | Document Description | | Rev X2 |
| CPU VTT POWER | | | |
| Date: | Sheet 48 of 63 | | |

V1P05PCH_CNTRL_INPUT
V1P8_CNTRL_INPUT

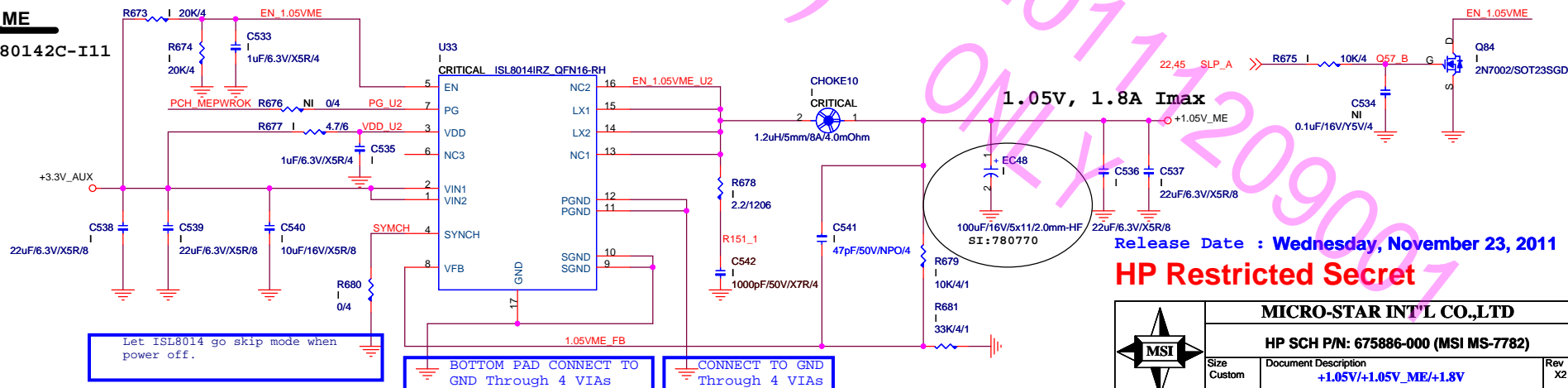


PCH_MEPWROK



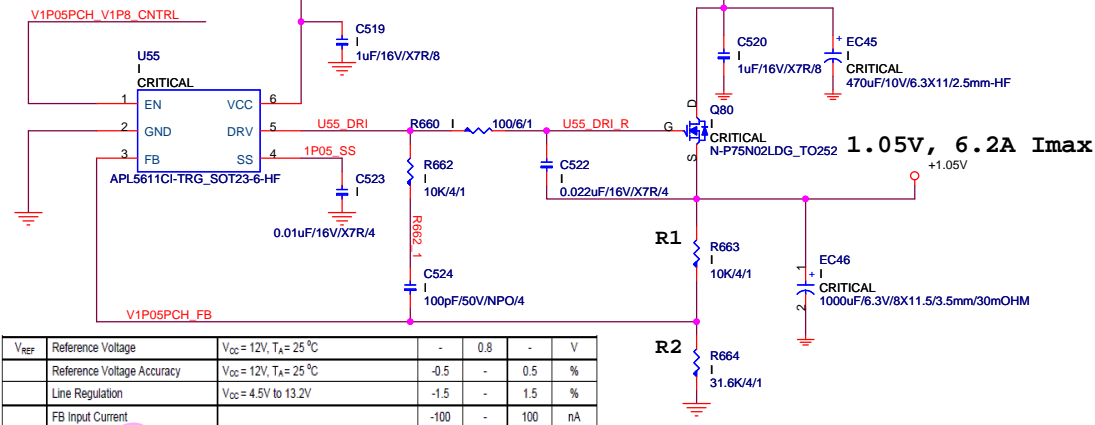
+1.05V_ME

PN:I32-080142C-I11



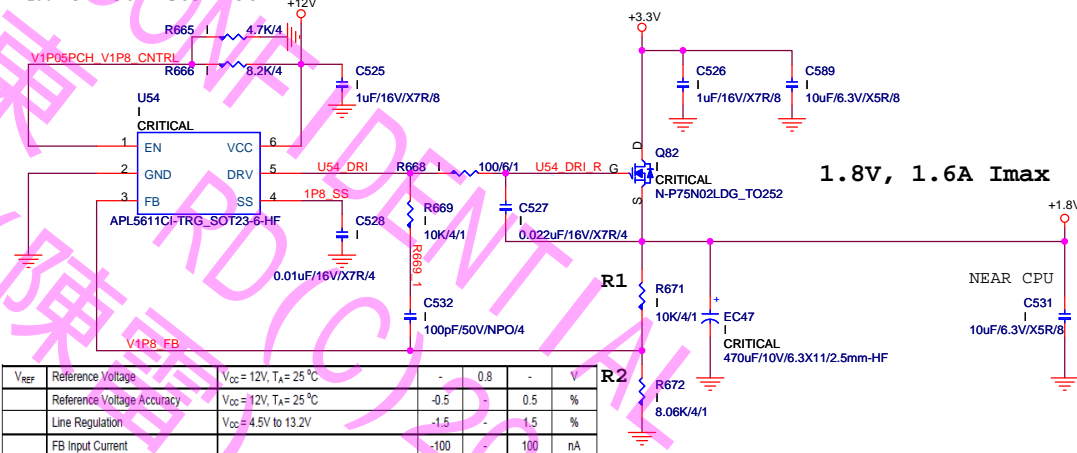
+1.05V

PN:I31-5611C09-A30



+1.8V

PN:I31-5611C09-A30



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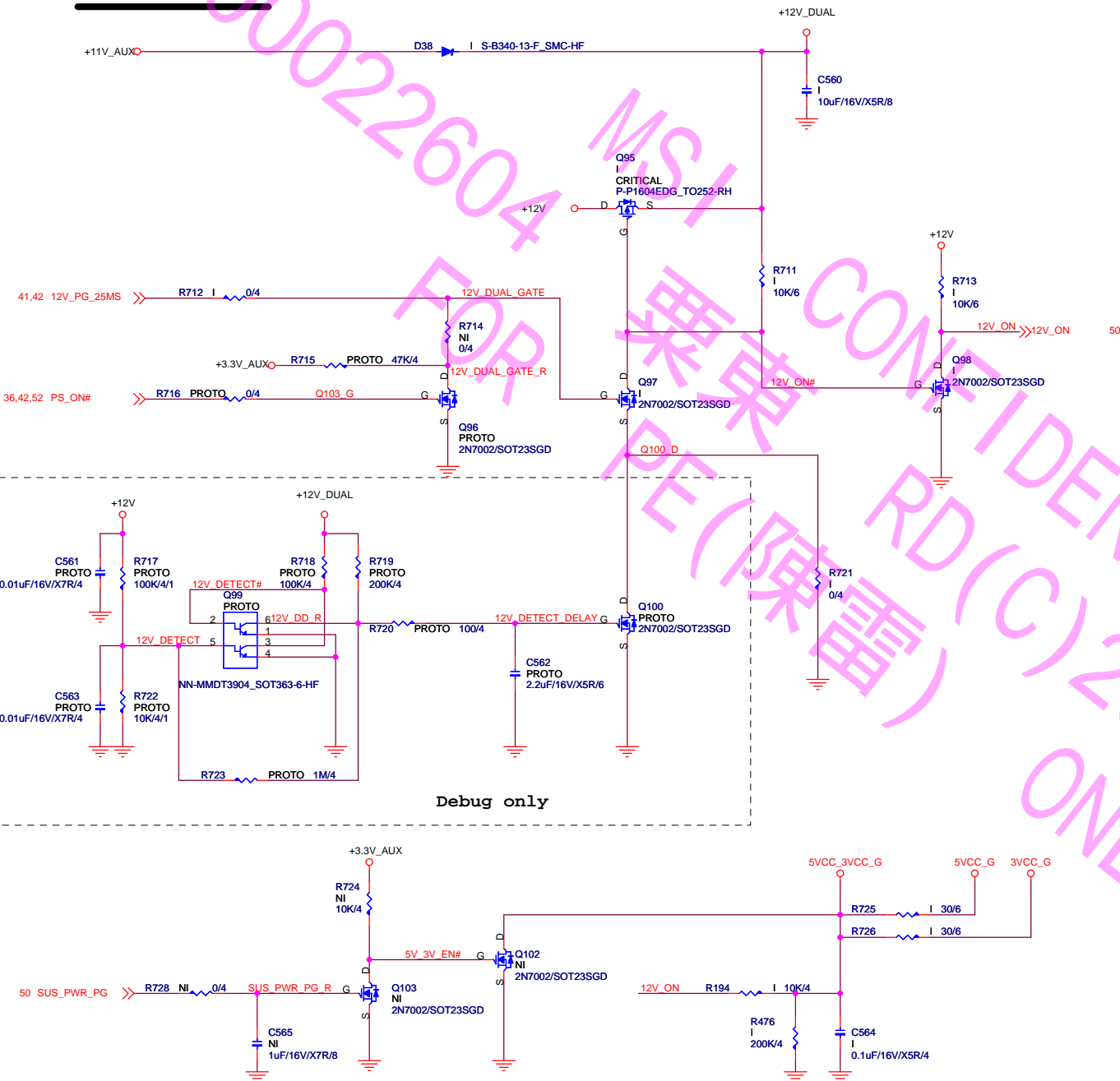


MICRO-STAR INT'L CO.,LTD

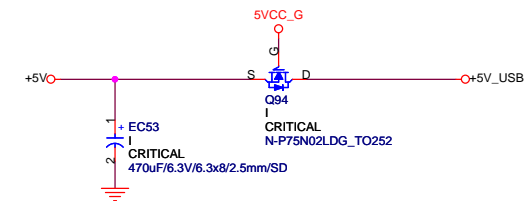
HP SCH P/N: 675886-000 (MSI MS-7782)

| | | |
|----------------|---|----|
| Size Custom | Document Description +1.05V/+1.05V_ME/+1.8V | Re |
| Date: | Sheet 49 of 63 | |

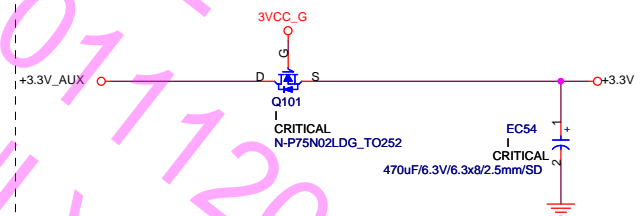
+12V_DUAL



+5V



+3.3V



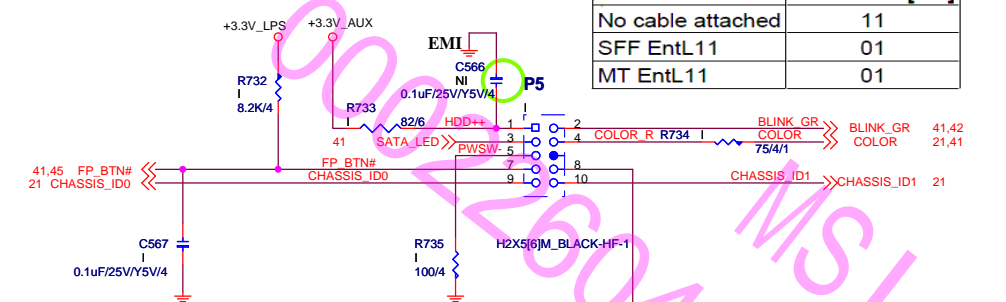
Release Date : Wednesday, November 23, 2011

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|---|--|-----------|
| MICRO-STAR INT'L CO.,LTD | | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description +12V_DUAL / +5V / +3.3V | Rev X2 |
| Date: _____ Sheet 51 of 63 | | |

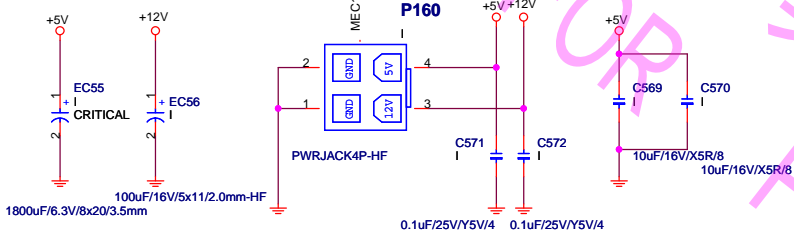
Front Panel

PN:N31-20510E1-F02



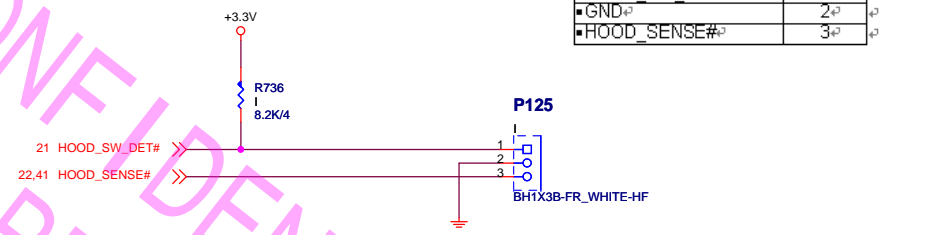
SATA POWER CONNECTOR

PN:N93-04M0451-H06



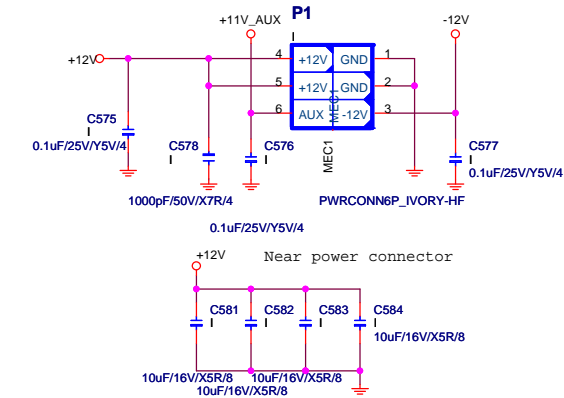
HOOD SENSE

N32-1030911-H06



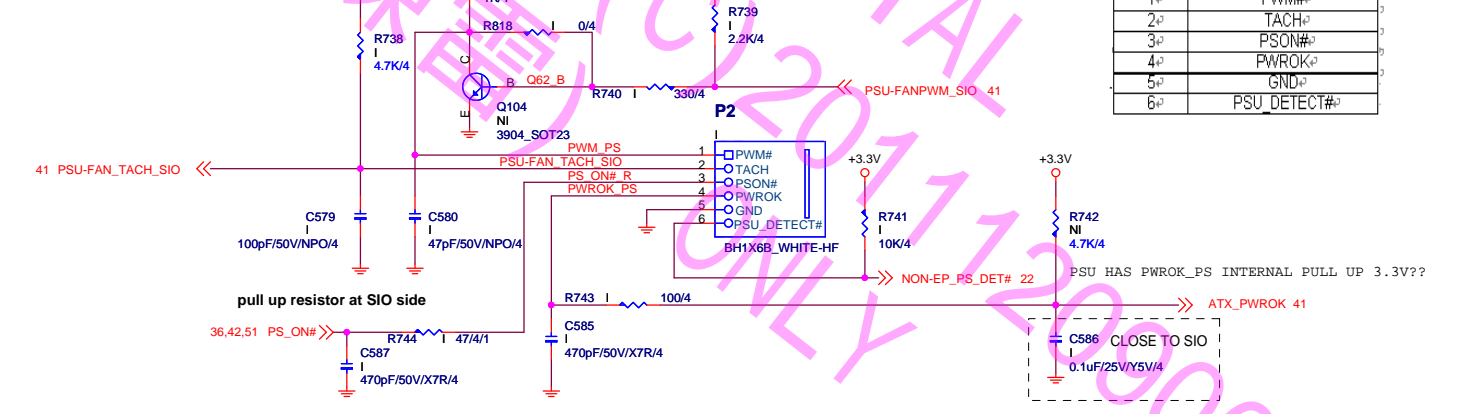
ATX Connector

PN:N93-06M0241-H06



PSU FAN

PN:N32-1060581-H06



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CPU XDP

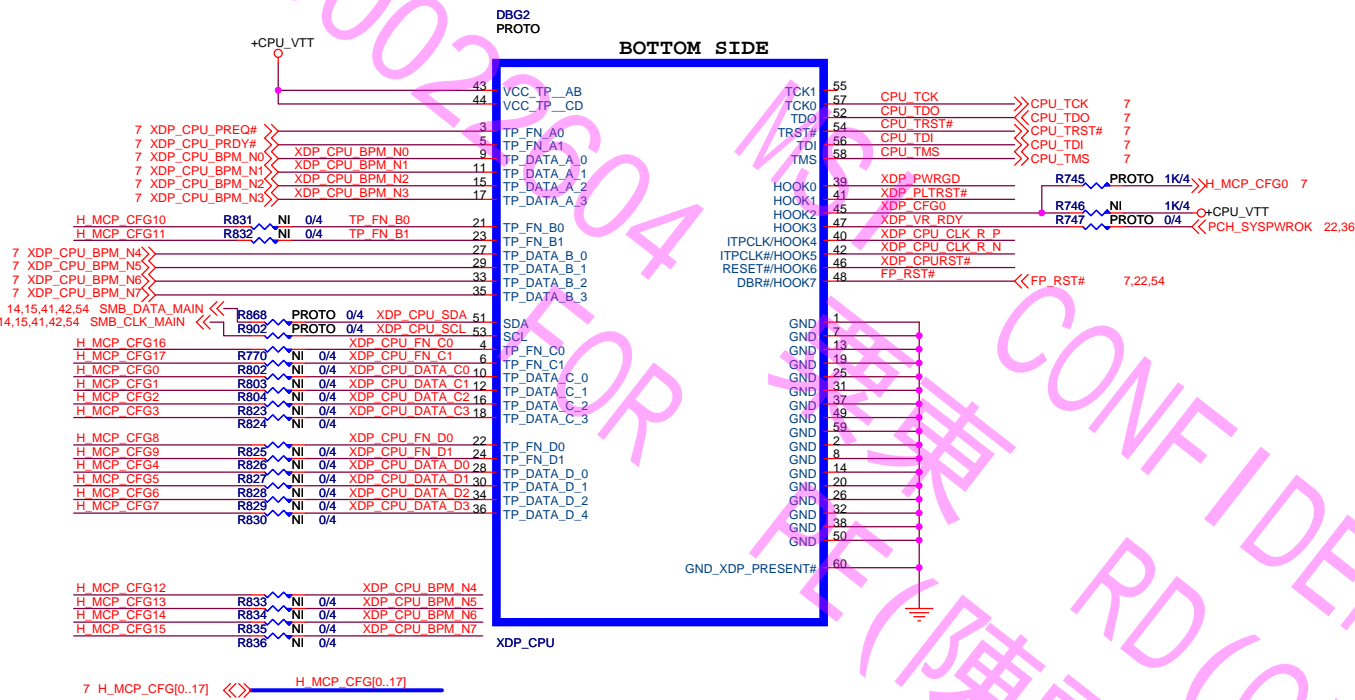
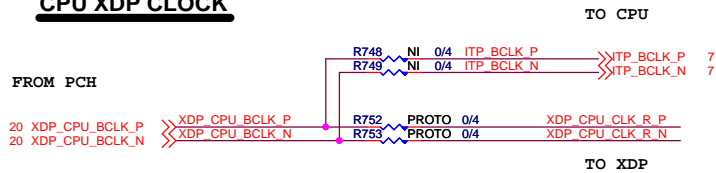


Table 3-1. Processor XDP Connector Pinout

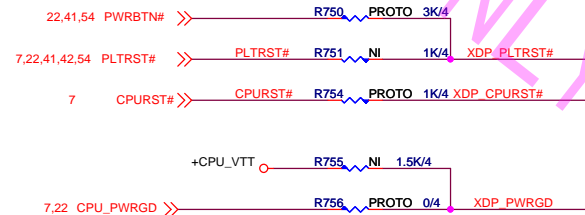
| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|-----|-------------------------|------------------------------|-----|-----------|-----|-------------------------|------------------------------|-----|-----------|
| 1 | GND | GND | NA | | 2 | GND | GND | NA | |
| 3 | OBSFN_A0 ¹ | PREQ# | I/O | processor | 4 | OBSFN_C0 ¹ | CFG[8] | I/O | processor |
| 5 | OBSFN_A1 ¹ | PRDY# | I/O | processor | 6 | OBSFN_C1 ¹ | CFG[9] | I/O | processor |
| 7 | GND | GND | NA | | 8 | GND | GND | NA | |
| 9 | OBSDATA_A0 ¹ | BPM#[0] / CFG[12] | I/O | processor | 10 | OBSDATA_C0 ¹ | CFG[0] | I/O | processor |
| 11 | OBSDATA_A1 ¹ | BPM#[1] / CFG[13] | I/O | processor | 12 | OBSDATA_C1 ¹ | CFG[1] | I/O | processor |
| 13 | GND | GND | NA | | 14 | GND | GND | NA | |
| 15 | OBSDATA_A2 ¹ | BPM#[2] / CFG[14] | I/O | processor | 16 | OBSDATA_C2 ¹ | CFG[2] | I/O | processor |
| 17 | OBSDATA_A3 ¹ | BPM#[3] / CFG[15] | I/O | processor | 18 | OBSDATA_C3 ¹ | CFG[3] | I/O | processor |
| 19 | GND | GND | NA | | 20 | GND | GND | NA | |
| 21 | OBSFN_B0 ¹ | CFG[17] | I/O | processor | 22 | OBSFN_D0 ¹ | CFG[4] | I/O | processor |
| 23 | OBSFN_B1 ¹ | CFG[16] | I/O | processor | 24 | OBSFN_D1 ¹ | CFG[5] | I/O | processor |
| 25 | GND | GND | NA | | 26 | GND | GND | NA | |
| 27 | OBSDATA_B0 ¹ | BPM#[4] | I/O | processor | 28 | OBSDATA_D0 ¹ | CFG[10] | I/O | processor |
| 29 | OBSDATA_B1 ¹ | BPM#[5] | I/O | processor | 30 | OBSDATA_D1 ¹ | CFG[11] | I/O | processor |
| 31 | GND | GND | NA | | 32 | GND | GND | NA | |
| 33 | OBSDATA_B2 ¹ | BPM#[6] | I/O | processor | 34 | OBSDATA_D2 ¹ | CFG[6] | I/O | processor |
| 35 | OBSDATA_B3 ¹ | BPM#[7] | I/O | processor | 36 | OBSDATA_D3 ¹ | CFG[7] | I/O | processor |
| 37 | GND | GND | NA | | 38 | GND | GND | NA | |
| 39 | HOOK0 | PWRGOOD | I | system | 40 | ITPCLK/HOOK4 | BCLK_ITP | I | processor |
| 41 | HOOK1 ¹ | BP_PWRGD_RST# | I | system | 42 | ITPCLK/HOOK5 | BCLK_ITP# | I | processor |
| 43 | VCC_OBS_AB | VTT Voltage of the processor | I | | 44 | VCC_OBS_CD | VTT Voltage of the processor | I | |
| 45 | HOOK2 | TAPPWRGOOD | I | processor | 46 | HOOK6/RESET# | RESET_OBS# | I | processor |
| 47 | HOOK3 | Open | NA | | 48 | HOOK7/DBR# | DBR# | O | processor |
| 49 | GND | GND | NA | | 50 | GND | GND | NA | |
| 51 | SDA ¹ | SDA | I/O | system | 52 | TDO | TDO | I | processor |
| 53 | SCL ¹ | SCL | I/O | system | 54 | TRSTn | TRST# | O | processor |
| 55 | TCK1 | Open | NA | | 56 | TDI | TDI | O | processor |
| 57 | TCK0 ³ | TCK | O | processor | 58 | TMS | TMS | O | processor |
| 59 | GND | GND | NA | | 60 | GND (XDP_PRESENT#) | -- | NA | |

1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed.

CPU XDP CLOCK



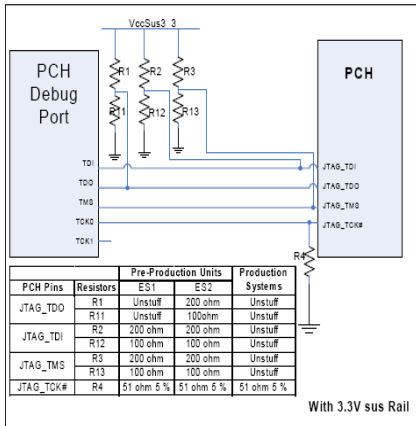
CPU XDP PWRGD/RESET



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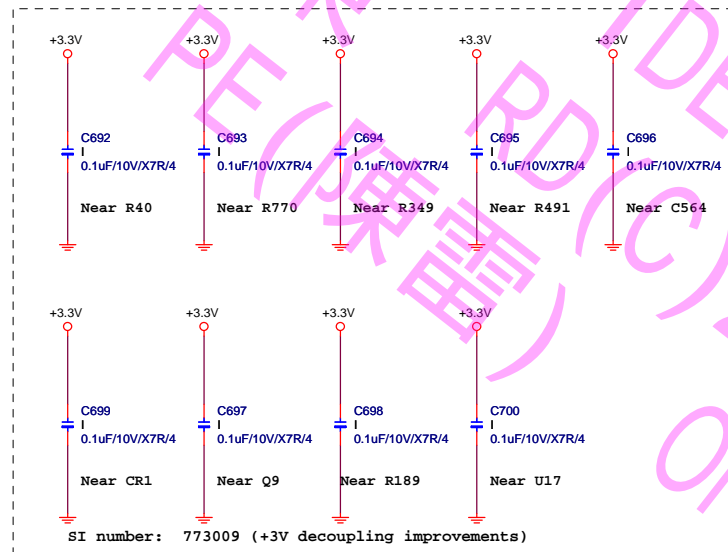
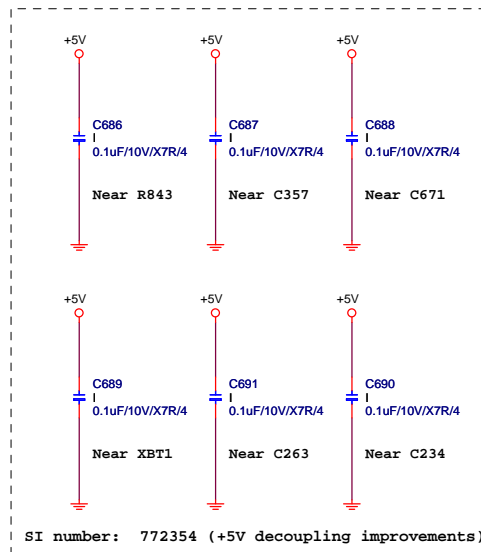
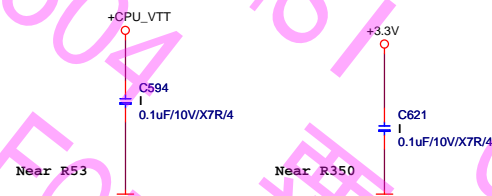
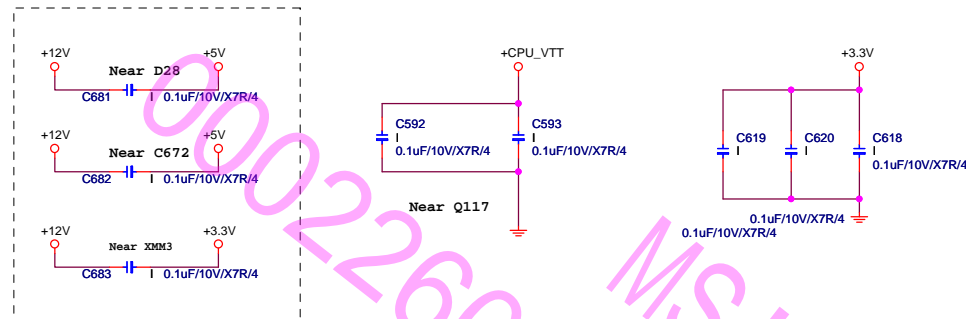
| | | |
|--------------------------------------|----------------------|--------|
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| HP SCH P/N: 675886-000 (MSI MS-7782) | | |
| Size Custom | Document Description | Rev X2 |
| CPU XDP | | |
| Date: | Sheet 53 of 63 | |

DBG3
PROTO

| | | Pre-Production Units | | Production Systems |
|-----------|-----------|----------------------|------------|--------------------|
| PCH Pins | Resistors | ES1 | ES2 | |
| JTAG_TDO | R1 | Unstuf | 200 ohm | Unstuf |
| | R11 | Unstuf | 100ohm | Unstuf |
| JTAG_TDI | R2 | 200 ohm | 200 ohm | Unstuf |
| | R12 | 100 ohm | 100 ohm | Unstuf |
| JTAG_TMS | R3 | 200 ohm | 200 ohm | Unstuf |
| | R13 | 100 ohm | 100 ohm | Unstuf |
| JTAG_TCK# | R4 | 51 ohm 5 % | 51 ohm 5 % | 51 ohm 5 % |

| | |
|-------|----------------|
| Date: | Sheet 54 of 63 |
|-------|----------------|

For EMI



SI number: 772354 (+5V decoupling improvements)

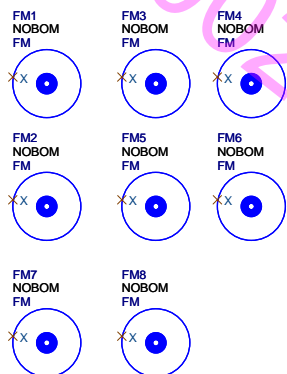
SI number: 773009 (+3V decoupling improvements)

Release Date : Wednesday, November 23, 2011

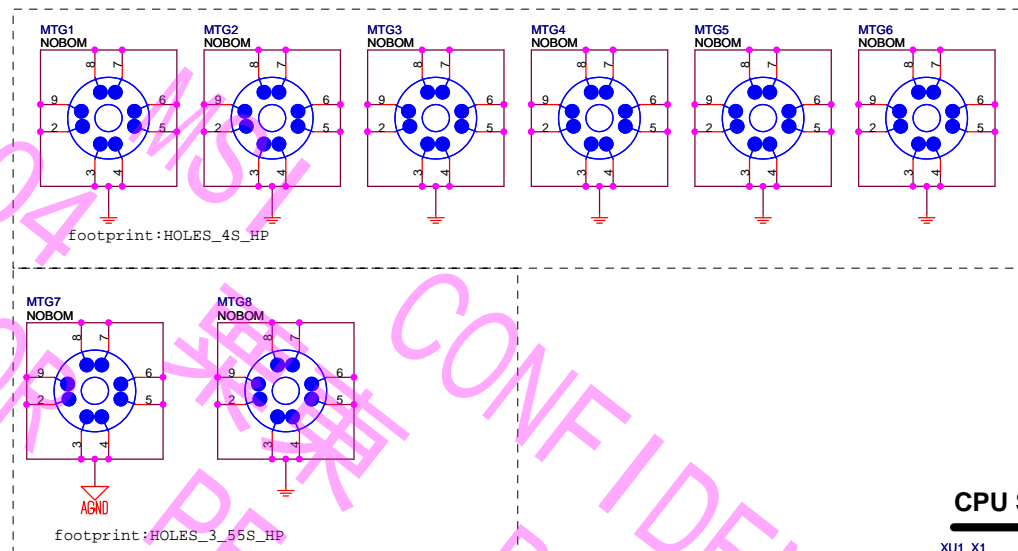
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|--------------------------------------|------------------------------|
| MICRO-STAR INT'L CO.,LTD | |
| HP SCH P/N: 675886-000 (MSI MS-7782) | |
| Size Custom | Document Description For EMI |
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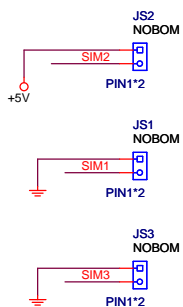
Optics Orientation Holes



Mounting Holes



Simulation



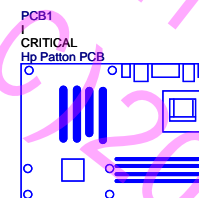
NB/SB FAN/HEAT-SINK



BATTERY

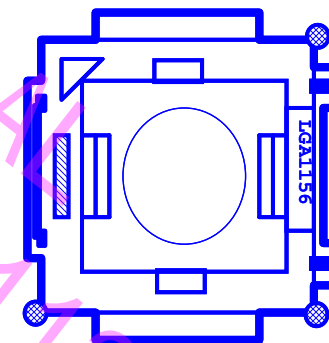


PCB




CPU SOCKET

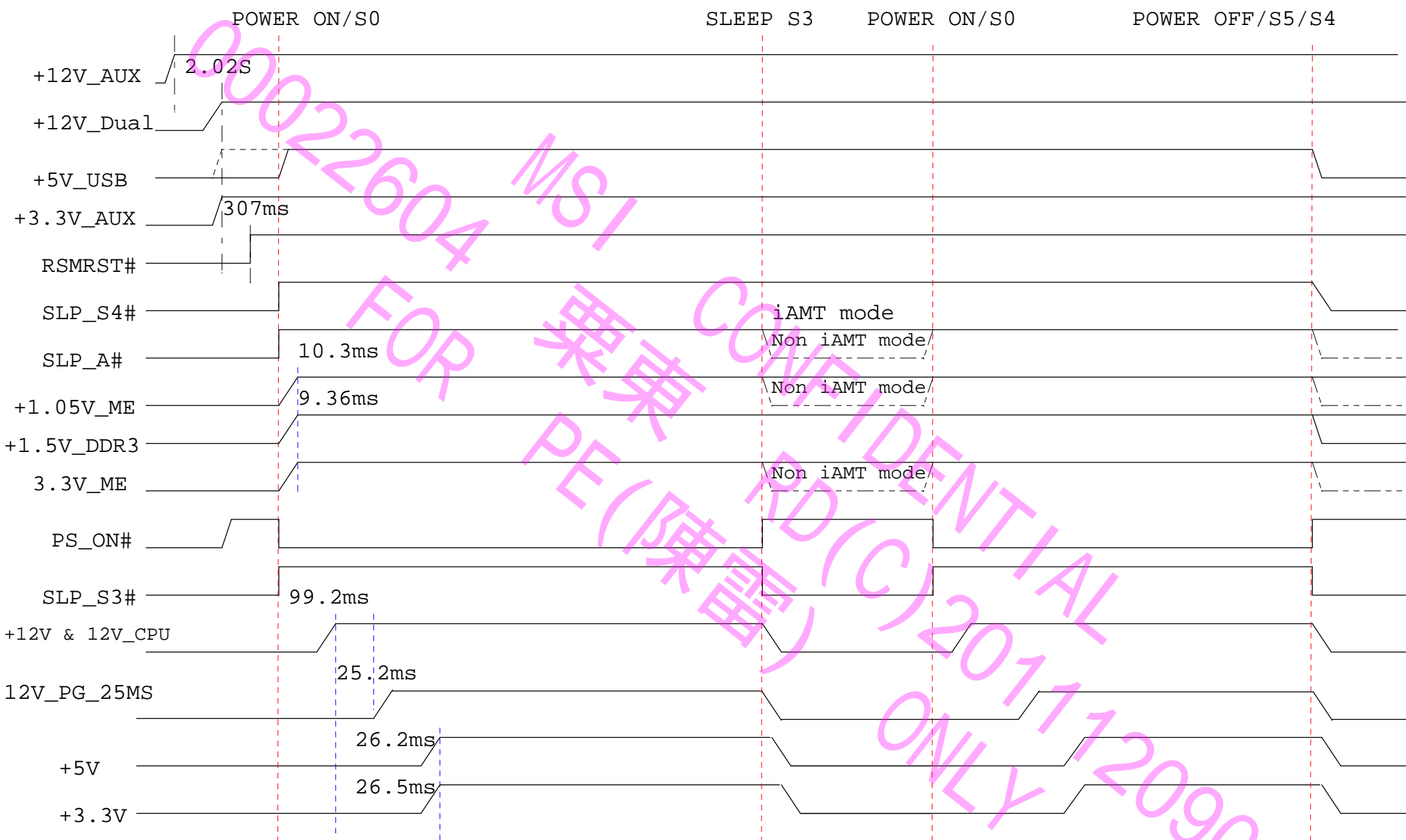
XU1_X1
CRITICAL
CPU SOCKET



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| | Size Custom | Document Description BOM - Option Parts | | |
| | Date: | | Sheet 56 of 63 | Rev |



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| | Size Custom | Document Description Power Sequence-1 | Rev X2 |
| | Date: | | Sheet 57 of 63 |


Voltage Sequence Timing Requirements



- Notes:**
- 1. T16 = Time required for VTT to reach 90% of its level before VSA is asserted.
 - 2. T17 = Time required for VTT to reach 90% of its level before VCCPLL is asserted.

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|---|---|--------------------------------------|--|
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PWRGD_30MS & SLP_S3# & CPU_SA_PG

| ATX P/S | | |
|---------|-------|----------|
| -12V | +12V | +12V_AUX |
| +/-5% | +/-5% | +/-5% |

| CPU PW | |
|--------|-------|
| 12V | +/-5% |

| VRD12 | |
|-----------|---------------|
| +CPU_VCCP | PWM REGULATOR |
| +CPU_GFX | PWM REGULATOR |

| +CPU_VTT PWM REGULATOR | |
|------------------------|--|
| PWRGD_30MS & SLP_S3 | |

| +1.5V_DDR3 PWM REGULATOR | |
|--------------------------|--|
| SLP_S4# | |

| +5V_USB PWM REGULATOR | |
|-----------------------|--|
| 5V_USB_EN | |

| +3.3V_AUX PWM REGULATOR | |
|-------------------------|--|
| LPS_ON# | |

| PCI Slot (per slot) | |
|---------------------|--------|
| +5V | 5.0A |
| +3.3V | 7.6A |
| +12V | 0.5A |
| +3.3Vaux | 0.375A |
| -12V | 0.1A |

| PCI Slot (per slot) | |
|---------------------|--------|
| +5V | 5.0A |
| +3.3V | 7.6A |
| +12V | 0.5A |
| +3.3Vaux | 0.375A |
| -12V | 0.1A |

| X1 PCIE per | |
|-------------|------|
| +3.3V | 3.0A |
| +12V | 0.5A |
| +3.3Vaux | 0.4A |

| X16 PCIE | |
|----------|------|
| +3.3V | 3.0A |
| +12V | 5.5A |
| +3.3Vaux | 0.4A |

| USB X2 IN | |
|-----------|------|
| +5V_USB | 1.0A |

| USB X4 FR | |
|-----------|------|
| +5V_USB | 2.0A |

| USB X4 RL | |
|-----------|------|
| +5V_USB | 2.0A |

| 2XPS/2 | |
|---------|------|
| +5V_USB | 1.0A |

| Sandy / Ivy Bridge (65W) | |
|-------------------------------|--|
| VCCP (CPU core 8 bit VID) 55A | |
| VAXG (GFX core) 25A | |
| VTT (CPU Uncore, I/O) 8.5A | |
| VSA (CPU system agent) 8.8A | |
| VccPLL (SFR supplies) 1.5A | |
| VDDQ (DDR I/O) 4.75A | |


| PCH H61 (5.5W) | |
|--------------------------|--|
| V_CPU_IO 1.05V .001A | |
| V5REF 5V .001A | |
| V5REF_Sus 5V .001A | |
| Vcc3_3 3.3V 0.409A | |
| VccADAC 3.3V 0.068A | |
| VccADPLLA 1.05V 0.1A | |
| VccADPLLB 1.05V 0.1A | |
| VccCore 1.05V 1.6A | |
| VccDMI 1.05V 0.057A | |
| VccIO 1.05V 4.07A | |
| VccSPI 3.3V 0.02A | |
| VccASW 1.05V 1.61A | |
| VccDSW3_3 3.3V 0.003A | |
| VccDFTREM 1.8V 0.2A | |
| VccRTC 3.3V 6uA | |
| VccSus3_3 3.3V 0.097A | |
| VccSusHDA 3.3V 0.01A | |
| VccVRM 1.8 0.159A | |
| VccCkDMI 1.05V 0.02A | |
| VccSSC 1.05V 0.105A | |
| VccDIFFCLKN 1.05V 0.055A | |

| HD Audio ALC 221 | |
|---------------------|--|
| +5V_AVDD/DVDD 41 mA | |
| +3.3V_DVDD 23 mA | |

| LAN BCM57788 | |
|-----------------|--|
| +3.3V_LAN 84mA | |
| +1.2V_LAN 333mA | |

| SUPER I/O SIO12 | |
|-----------------|--|
| +3.3V_AUX 20mA | |
| +3.3V 1mA | |
| VBAT 1uA | |

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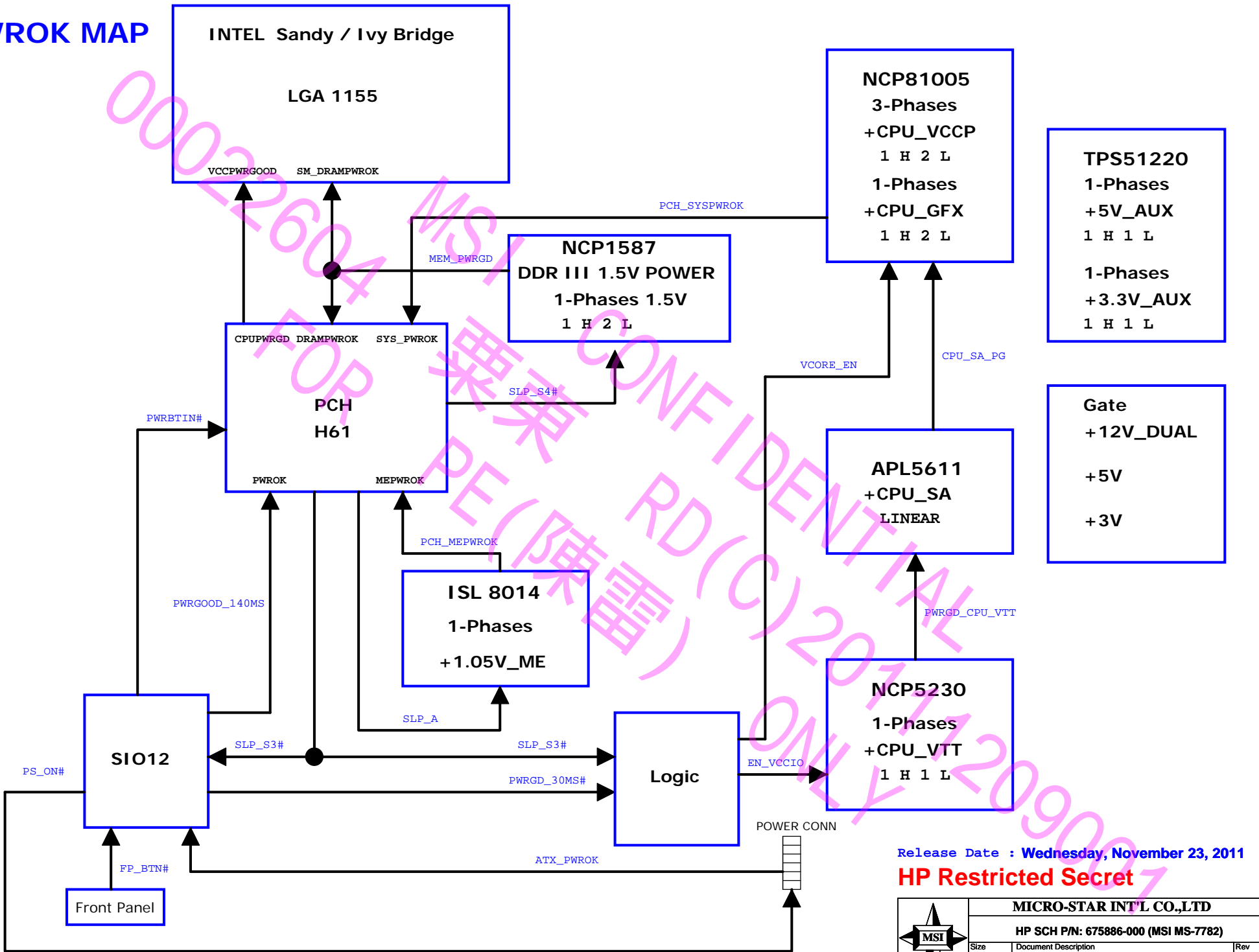


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| Size Custom | Document Description | Rev X2 |
| | Power Delivery | |
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PWROK MAP



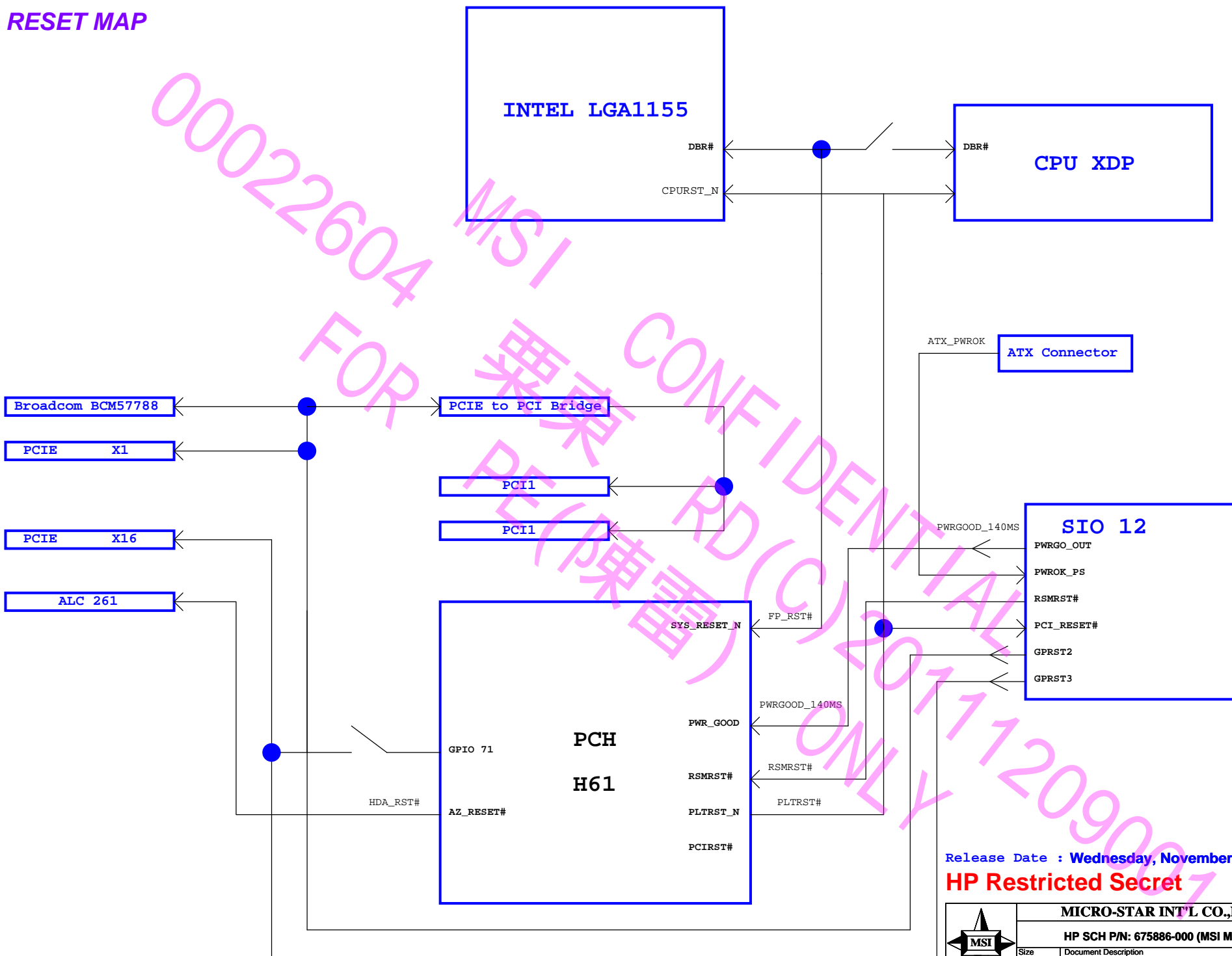
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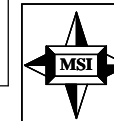
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|--------------------------------------|--------------------------------|--------|
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| Size Custom | Document Description PWROK MAP | Rev X2 |
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RESET MAP



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| | |
|--------|----------------------|
| Size | Document Description |
| Custom | RESET MAP |

| | |
|-----|---|
| Rev | X |
|-----|---|

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|-------|----------------|
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Patton OA

2011/09/01 MS-7782 OA START

2011/09/27 MS-7782 OA Gerber Out

2011/09/30

PAGE55:+5V decoupling improvements (SI number: 772354)

PAGE55:+3V decoupling improvements (SI number: 773009)

2011/10/21

PAGE14,15:Data Mask has to connect to GND (SI number: 777180-2)

PAGE18:Modify DMI TX/RX circuit (SI number: 777197)

PAGE23:Modify DVI circuit (SI number: 777225)

PAGE36:XU19 pin5 must be connected to the E16 Pin 3 because SPI BOM can not be readed data (SI number: 777160)

2011/11/03

PAGE32:UUT is unable to power on if battery is removed;C240 is changed from 1uF to 4.7uF(SI number: 778258)

2011/11/10

PAGE13:- Modify Patton CPU power circuit to meet Intel CPU power transient test; C10,C11 have been changed from NI to I.(SI number: 780343)

PAGE46:- Modify Patton CPU power circuit to meet Intel CPU power transient test; C417=>220pF,R566=> 3.3K,R584=>7.15K,C443=>1500pF,C442=>820pF,R587=>8.66K (SI number: 780343)

PAGE47:- Modify Patton CPU power circuit to meet Intel CPU power transient test;EC34=>470uF (SI number: 780343)

PAGE48:- Modify Patton CPU power circuit to meet Intel CPU power transient test;C508=>0.01uF,C509=>0.01uF,C505=>2200pF,R629=>3.6K (SI number: 780343)

2011/11/14

PAGE33:Patton EVT1 RGB signals rise/fall time and pk-pk noise don't meet VESA 1.2 spec ;C246,C249,C252 have been chngne from 2.7pF to 4.7pF;L9~L14 have been changed from 33nH to 47nH. (SI number: 778268)

PAGE49:Add a 100uF cap to +1.05V_ME power;EC48 =>100uF (SI number: 780770)

PAGE50:system power 3.3V change current to 22A solution ;Q86 =>MFS4921*1,Q87=>MFS4937*2 ,CHOKE12 => 1.5uH.EC52 => CAP SOLID,470uF*2,R690 => 7.15K ohm,R687 => 15.8K ohm,EC49 =>,CAP SOLID,100uF (SI number: 780766)

2011/11/16

PAGE28:LAN_AVDDL decoupling improvement;added C342,C343 near U10 pin 27,33 (SI number: 783475)

2011/11/17

PAGE42:Add LPC Debug Header;Added E17 (SI number: 780764)

PAGE42:SIO12 schematic review,strap pins pull down resistor value should be ;R879,R880,R881 have been changed to 4.7K ohm (SI number: 784070)

2011/11/21


PAGE13:Intel feedback "Some of the power decoupling caps (value and Qty) are not following Intel's recommendation " ,added 10uF :351,C352,C455,C456,C457,C458 (SI number: 784909)

PAGE24:Intel feedback "Some of the power decoupling caps (value and Qty) are not following Intel's recommendation " ,added 1uF:C701 (SI number: 784909)

PAGE47:Intel feedback "Some of the power decoupling caps (value and Qty) are not following Intel's recommendation " ,added 10uF:C344,C345,C347,C348; 270uF:EC38 (SI number: 784909)

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| | Size Custom | Document Description HISTORY-1 | Rev X2 |
| | Date: | Sheet 63 of 63 | |